Quality Assurance and Control for the ProtoDUNE-SP Photon Detector Readout Electronics

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1 Introduction

This document describes procedures used for the quality assurance and subsequent quality control procedures for the prototDUNE-SP photon detector readout electronics, so-called SSP (SiPM Signal Processor) Boards.

ANL HEP Neutrino Group is responsible for the development, fabrication, testing, integration, and commissioning of the ProtoDUNE-SP photon-detector readout system. Some of these responsibilities are shared with other ProtoDUNE-SP photon-detector groups within collaboration. In covering these tasks the areas responsibility of the group went from the development of the readout system tested and operated in recent 35-ton detector to develop a new design and fabricate system to meet the ptotoDUNE-SP photon-detector readout system requirements. These activities involved modifications in power supply solutions, re-definition of trigger/timing interface to the readout electronics (SSP), formation of trigger output from SSPs, firmware modifications in data readout mode and data format, and changes the SSP data output interface. The SSP design and interfaces will be described in separate documents and drawings [1], [2], [3].

Photon detector system components will be acquired or manufactured at various institutions throughout the photon group. As described in the overall photon-detector quality assurance and control plan [4], each institution will develop a quality assurance program for the system components in area of group's responsibility, leading to a corresponding set of quality control requirements and procedures.

2 Photon Detector Readout Electronics QC Procedures

We identify two levels of testing for the SSP, summarized as follows:

1. **Post-assembly Testing** is used by ANL personnel to perform engineering-level tests required to verify that a newly-assembled SSP works well enough to proceed to characterization & calibration testing.
2. **Characterization Testing** is performed by ANL personnel using a "standard" detector and/or "standard" signal generators to perform a series of performance measurements on a fully-functional SSP module, before delivery for ProtoDUNE at CERN.

Additionally, after delivery of any SSP unit to ptotoDUNE, additional tests shall be performed at CERN. These additional tests are beyond the scope of this paper, although summary descriptions are provided in section 4. These additional test regimes include Vertical-Slice testing, Integration testing and Installation testing.

The QA/QC repository of identified quantities of interest may include the following:

- board_sn

- channel_number
- sipm_sn
- test_trace_image
- bias_voltage
- threshold
- dark_rate
- gain
- cross_talk
- pre_test_photo
- comments
- create_time
- create_user
- update_time
- update_user

It is expected that at each level of testing some but not all of the universe of QA/QC parameters will be measured. Table 2 correlates fields from the list above to the test levels at which the fields are expected to be recorded and/or measured.

	Post-Assembly	Characterization	Vertical Slice	Integration	Installation
board_sn	Y	Y	Y	Y	Y
channel_number	Y	Y	Y	Y	Y
sipm_sn	N/A	Y	N/A	Y	Y
test_trace_image	Y	N/A	Y	Y	Y
image	N/A	N/A	N/A	Y	Y
bias_voltage	Y	Y	Y	Y	Y
threshold	Y	Y	N/A	Y	Y
dark_rate	N/A	Y	N/A	Y	Y
gain	Y	Y	N/A	Y	Y
cross_talk	Y	Y	N/A	Y	Y
pre_test_photo	N/A	N/A	N/A	Y	Y
comments	Y	Y	Y	Y	Y
create_time	Y	Y	Y	Y	Y
create_user	Y	Y	Y	Y	Y
update_time	Y	Y	Y	Y	Y
update_user	Y	Y	Y	Y	Y

Table 1: QA/QC test sorted by testing category.

Details and illustrations of post-assembly tests are provided in "DUNE SiPM Signal Processor Procedure" document [5]. Separate test procedure documents are maintained for post-assembly and characterization tests performed at ANL.

2.1 Post-assembly Testing

Post-assembly testing uses DUNEWare, run on a PC in appropriate lab space. Post-assembly testing is itself sub-divided into two subsections:

1. **PRE-SOFTWARE tests** are at the level before the board may communicate with a PC and are manual in nature. A computer-based "checklist" screen walks the user through each step, asks for input as needed (or a simple "OK" button), and saves the data into a time- and date-stamped test record file.

   These tests will include the following:

   (a) Verify that the mechanical assembly is complete.

   (b) Measure all power supplies (unpowered) to check for shorts/opens.

   (c) Measure current/voltage draw of un-programmed SSP (all supplies).

   (d) Check fans and LEDs.

   (e) Check switching frequencies of DC-DC converters.

   (f) Load firmware and verify correct programming. This is done through JTAG, not the Ethernet interface.

   (g) Re-measure current/voltage draw of programmed SSP (all supplies).

   A summary statement that all assembly, basic power supply function and programmability are correct within specifications is noted in the QA/QC documentation for each module.

2. **SOFTWARE-mediated tests** exercise the board by running specific test programs. Each of these programs performs a series of measurements/tests, calculates parameters and develops a pass/no-pass response. The measurements, results, parameters and pass/no-pass result are logged to the time- and date-stamped test record file. Each test will have its own pop-up window to prompt the user for any external hardware setup or human confirmation of activity (e.g. LEDs).

   The tests foreseen are:

   (a) Verify basic communication. Record firmware IDs as read from devices.

   (b) Blink LEDs and check status counters through Ethernet control.

   (c) Exercise TRIG OUT function using manual control.

   (d) Check alignment of ADC clocks and data bits.

   (e) Check analog DC offsets and noise levels with no inputs.

   (f) Verify integrity (polarity & shielding) of all input connections.

   (g) Exercise monitoring ADCs.

   (h) Verify bias voltage operation.

   (i) Use internal charge injection circuit to perform coarse gain/offset/noise measurements for each channel.

   (j) Compare charge injection results versus pulse generator test signal applied to each channel.

   (k) Verify operation of timing interface (if provided by Timing Group).

   The recorded timestamp in the SSP and distribution of timestamp values for a series of events in which a test pulse occurring at regular timestamp intervals T1, T2, T3, etc. is noted in the QA/QC documentation.

Software derived from the existing DUNEWare engineering test program will be used. A "non-expert" screen enumerating only the list of tests above will be presented. The user will click a button to start each test, and will be prompted as needed to walk the user through the test. The time- and date-stamped log file will contain all required QA/QC information for the board in both summary (pass/no-pass, number of test cycles, log of repairs (if any), etc.) and detailed versions (charge injection test results).

A summary checklist of functional tests demonstrating that a module has passed all main checkpoints of **Post-Assembly testing** is stored for overall QA/QC documentation. Detailed electronic records of every step of post-assembly testing, including how often any given SSP module has been cycled through post-assembly testing and any modifications to said module that may occur shall be recorded and archived separately. The general method that shall be used at Argonne for post-assembly testing and characterization will be to use time- and date-stamped files, one generated each time the test software is run. Each file's name shall encode the time and date when the file was generated, and the files shall be stored in a hierarchical folder structure where the folder name indicates which serial number/version of SSP is tested.

2.2 Characterization Testing

Characterization testing measures the performance of an SSP module under various end-use scenarios, saving appropriate records of each test into the QA/QC documentation. A module only enters the Characterization sequence if it has previously passed the post-assembly sequence. Characterization testing is not intended to determine whether a module is usable or not, but rather to more carefully measure the performance of each functional module.

Grounding of each setup is extremely important and thus a checklist of connections is required for each step. Also as in post-assembly testing, the responses of the user are recorded in a time- and date-stamped file for quality assurance purposes.

The various tests foreseen for this level of testing include the following:

1. Measurement of DC offset and RMS of every channel. Check for presence of noise.
   (a) With no cables connected to SSP inputs to measure baseline offset/rms).
   (b) With a cable connected to each of SSP inputs.
   (c) With warm unbiased SiPM with cable connected to each of SSP inputs.
   (d) With warm biased (below breakdown voltage) SiPM with cable connected to each of SSP inputs.
   (e) With cold biased (above breakdown voltage) SiPM with cable connected to each of SSP inputs.
   (f) With cold biased SiPM with cable connected, through feedthru (if available) to each of SSP inputs (test of noise in experiment-equivalent setup).
2. Measurement of gain of every channel using external charge pulse generator
   (a) With cable from a pulse generator to each of SSP inputs. Generate a charge 'blob" to measure channel gains.
   (b) With cable from a pulse generator (in place of warm SiPM detector), through flange board (if available), to each of SSP inputs.
   (c) Measurement of full photoelectron spectrum (statistics of ADC counts per photo-electron) from every channel when connected to a cold detector through the full cable including flange board (if available). A flasher such as the 35t calibration module or a commercial pulse generator is used to generate light pulses. Such test will also determine the charge resolution of the readout system.

3 Relationship of Post-assembly and Characterization testing to protoDUNE QA/QC criteria

Post-assembly and Characterization testing will initially use pass/fail limits based upon the observed distributions of the QA/QC measurement parameters in previous setups such as the 35T test runs at Fermilab. The pass/fail limits shall be set conservatively such that modules passing both Post-assembly and Characterization testing at ANL should have reasonable expectation of operating within all protoDUNE QA/QC criteria. Due to the environmental differences between test stands and experiments (grounding, noise, power quality, temperature variation, etc.) there is no guarantee that may be expressed or implied for module performance in Vertical Slice, Integration, Installation or any other use case at CERN.

Instead, it is expected that the protoDUNE initial QA/QC criteria will, similarly to the Post-assembly and Characterization criteria, be based upon practical experience gained in previous setups such as the 35T test runs, and that such criteria will slowly evolve as operational experience is gained with the CERN environment. As the evolution of protoDUNE QA/QC criteria occurs, a formal feedback process is required to communicate requests for changes to the pass/fail limits applied in Post-Assembly and Characterization and to record in all QA/QC databases both at protoDUNE and at ANL when/if any such changes in pass/fail criteria take effect.

4 Photon Detector Readout Electronics Procedures at Integration and Installation stages

We briefly summarize tests to be performed at CERN. These additional tests are beyond the scope of this paper, and will be described in separate documents related to photon-detector integration and installation efforts at CERN.

1. **Vertical-Slice Testing** is a specific set of tests performed at CERN, on the first DUNE SSP only. The purpose of Vertical Slice Testing is to ensure that the SSP, the trigger system and the timing system all work with each other, all under the control of ArtDAQ, but does not include any characterizations with the rest of photon-detector system.

2. **Integration Testing** is performed at CERN, on a subset of the full photon detector. In integration testing a set of four SSPs (and the calibration module, if available) operate as expected when connected to photon detector units mounted within APA frame. The APA with photon-detector photo-sensors and light-collection bars, and photon-detector cables are located in a cold gas argon and read-out via the flange board. The SSPs operate with full interfaces to both trigger and timing systems. It is performed with the Cold Box setup, in a proximity to ProtoDUNE cryostat. The Cold Box integration tests start with the APA preparation in the clean room: photon-detector units are installed into APA frame; photon-detector cables are installed next; APA cold-electronics components with cables are installed next; the APA frames go into the Cold Box for integration testing and then directly into the cryostat. For the photon-detector it means that the same cables move from the Cold Box to the cryostat.

3. **Installation Testing** is performed at CERN after the photon-detector components are installed in protoDUNE cryostat. It is using the experiment DAQ to read out groups and/or all the SSPs of the photon detection system and verify that the PD system works as a whole, and demonstrate there is no interference with other detector subsystems.

References

[1] [DUNE Collaboration] ProtoDUNE-SP Techical Design Review, DUNE docdb-1794.

[2] J. Anderson, Z. Djurcic, G. Drake, M. Oberling et al., SSP Trigger and Timing Interface (under preparation).

[3] J. Anderson, Z. Djurcic, G. Drake, M. Oberling et al., Photon Detector System Cabling and Feedthru (under preparation).

[4] N. Buchanan et al, Quality Assurance and Control for protoDUNE Photon Detectors.

[5] J. Anderson, Z. Djurcic, G. Drake, M. Oberling et al., DUNE SiPM Signal Processor Procedure (under preparation, original document written for DUNE 35-ton SSPs).