ProtoDUNE SiPM Signal Processor

Revision A

May 04, 2017

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Size: Custom	Document Number: <Doc>		Rev: B
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Board and circuit changes AS APPLIED TO PC BOARD

Part Value changes

<OrgName>	
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	<Title>
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D	<Doc>
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<RevCode>

ADDED on 4-21-2017

MCO# 1 Top shield is to close to component pads reduce folded length to .5" from .6"

MCO# 2 Bottom and top shield interfer with front spacer. Reduce shields width to 3.915" from 4.0"

MCO#3 Use thinner or round standoffs to mount U255 (Zicor) hex ones interfer with mounting holes.

MCO# 4 Fans need to be tapped for a 6-32 binder head screw before mounting.

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DESIGN IMPROVEMENT PLANS

DIP #1) Unused pins GTP blocks of Artix-7 FPGA not tied to ground as recommended. No modification to assembled boards.
DIP #2) U275-1 and U276-1 should not be hard-tied to voltage.
a) Should have light pulldown resistors to GND and 'DNI' resistors to input voltage.
b) Desired operation is board defaults upon initial assembly to disabling both U275 and U276.
c) Would not hurt to have similar resistor setups for U272 and U286 as well.
DIP #3) Missing test point for +1.4V-post-filter and missing test point for +1.8V_A.
a) In general should have test points for all pre- and post-filter points to allow for measurement when inductors are out (immediately after assembly).
DIP #4) SM_JUMP3s implemented incorrectly. Resistors noted as laying inside SM_JUMP3s are adjacent to SM_JUMP3s.
a) related : default positions of overlaid resistors often incorrect. Fix.
b) Does not affect functionality of current board. Cosmetic only.
c) If keeping the SM_JUMP3, need to have consistent labeling between PCB and schematic as to which side is which. Easiest method would be to change schematic symbol to match PCB.
DIP #5) Boot-strap start-up use of MIO pins not properly noted in schematic. Add notes.
a) MIO 0 – OK – Supply pullup option only, via 20k. (10k is ok too.)
b) MIO 1 – OK – Supply pullup option only, via 240 ohm.
c) MIO 2 – CHANGE – Supply pullup and pulldown option. Load pullup pulldown with 20k.
d) MIO 3 – OK – Supply pulldown option only, via 20k.
e) MIO 4 – CHANGE – Supply pulldown option only, via 20k.
f) MIO 5 – CHANGE – Supply pullup option only, via 20k.
g) MIO 6 – OK – Supply pulldown option only, via 20k.
h) MIO 7 – CHANGE – Supply pulldown option only, via 20k.
i) MIO 8 – CHANGE – Supply pulldown option only, via 20k. Additionally see sketch of modified MIO 8 circuit below. (Same as ECO 3C.)

DIP #6) Insufficient part specified for U285; should have been Si5340 instead of Si53340. No modification to assembled boards. Fix in next design pass.
a) Would suggest Si5317 as an alternative to the Si5340. Part is pin programmable and already exists in design. Loop bandwidth can be set as low as 116Hz @ 250MHz. Has two outputs.
DIP #7) Per assembler, all the through-hole test points (AGND, DGND, VTxxx, etc.) are not correctly matched to hole size required by component. Need to increase size of holes.
DIP #8) Per assembler, paste file for U93, U285, U257, U273 has incorrect screening for ground connections.
DIP #9) Add secondary washing with degreaser into assembly specification. Wash provided in prototype assembly insufficient as some visible/tactile residue remains.
DIP #10) Silkscreen for next revision should explicitly label all resistors that tie to standoffs by which "ground" they tie to (e.g. DGND, AGND, PWRGND).
DIP #11) Bottom shield screws at 2-56 size are too small. Change in next revision to 4-40 and use threaded 4-40 spacers. Use of threaded spacers allows screws to be captured by bottom shield, simplifying assembly of shield.
DIP #12) Re-check the vertical orientation of the rectangular cutout on the back panel for the dual SFP connection to ensure that the gasket is appropriately considered.
DIP #13) Silkscreen for Vicor power supply U255 is reversed text.
DIP #14) When implementing ECO #7 in schematic, preserve U279, but replace with single diode.
DIP #15) Temperature measurements of operating board show two hot spots that should be addressed.
1. The –V_A linear regulator (LT3015) runs at 40 C with FPGAs programmed but not pushing data in closed box with fans on. According to Linear Tech thermal resistance table no difference in theta-ja for TO-220 versus DDPAK (both rated 34C/watt).
 Either way, needs a heat sink. Not dumping enough heat into board. Probably better with TO-220 as heat sinks are less goofy.
2. The Vicor DC-DC converter, under the shield box and with the fans on, also gets to about 40 C. Should modify mechanics of shield so that metal plate of Vicor can dump heat to top shield plate.
DIP #16) Silkscreen on backside of PCB for UZ1 and U277 is not aligned properly to vias.

DIP #17) Silkscreen on backside of PCB for U259 is missing.
DIP #18) Connect LOS output of U256 to Artix FPGA.
DIP #19) Consider hardware contolled power/bias LED.
DIP #20) Add voltage regulator and/or power monitor to generate two LED outputs : Bias Present and Bias OK. Bias Present should illuminate at as low a voltage as possible, Bias OK only when Vbias is within acceptable range (i.e. 34.0 – 34.2V).
DIP #21) Add requested external flip-flop to sample data from CDR.
DIP #22) As with DIP #20, there should also be Power Present and Power OK LEDs where PowerPresent means the Vicor is on and making 5V, Power OK means that in addition all secondary voltages are within tolerance.

<OrgName>			
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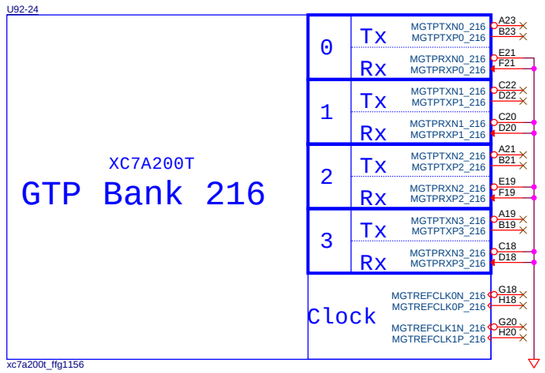
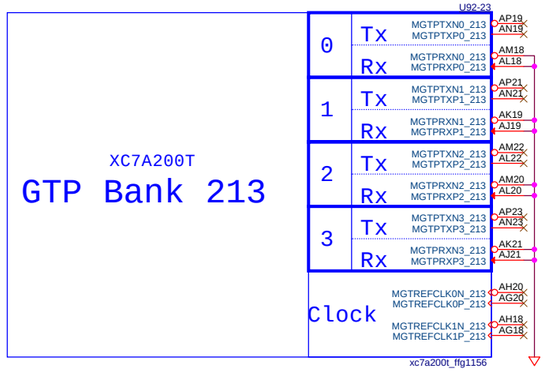
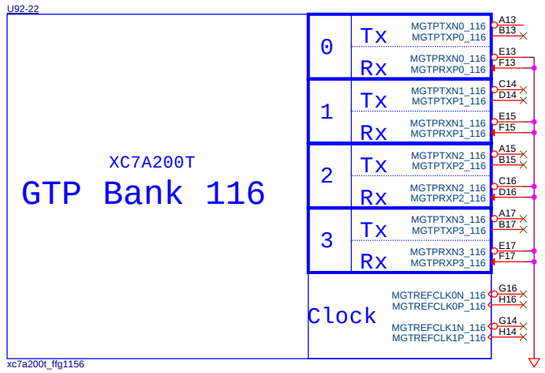
U1
DSP FPGA

DIP #1) Unused pins GTP blocks of Artix-7 FPGA not tied to ground as recommended.







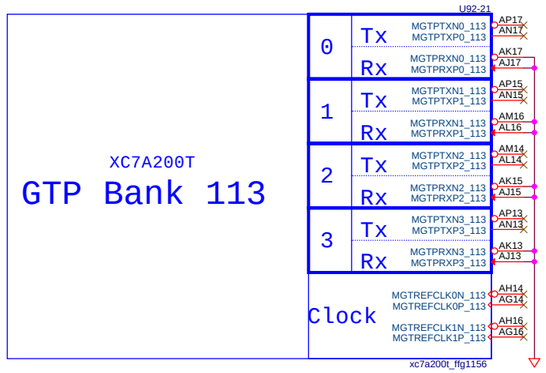
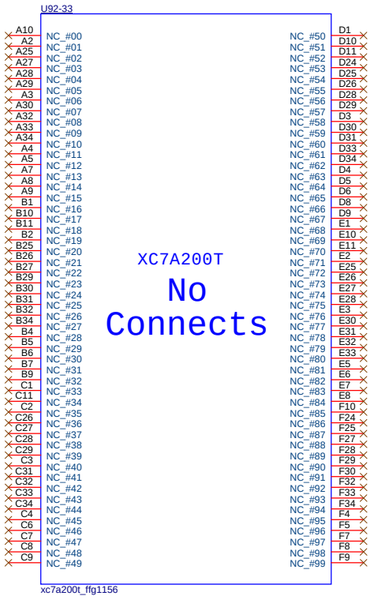


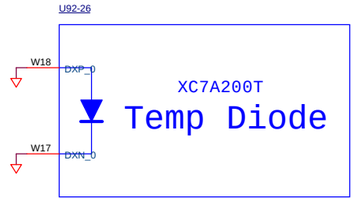
Table 5-4: **Unused GTP Quad Column Connections**

Pin or Pin Pair of the Unused GTP Quad	Connection
MGTAVCC	GND
MGTAVTT	GND
MGTREFCLKP/MGTREFCLKN	Float
MGTRXP/MGTRXN	GND
MGTTXP/MGTTXN	Float
MGTRREF[1]	GND

Notes:

1. This is the only scenario when the MGTRREF pins can be connected to ground. In all other scenarios, these pins must be connected for normal operation.





piece of fpga released from deletion of NOvA timing interface

Title	No Connects		
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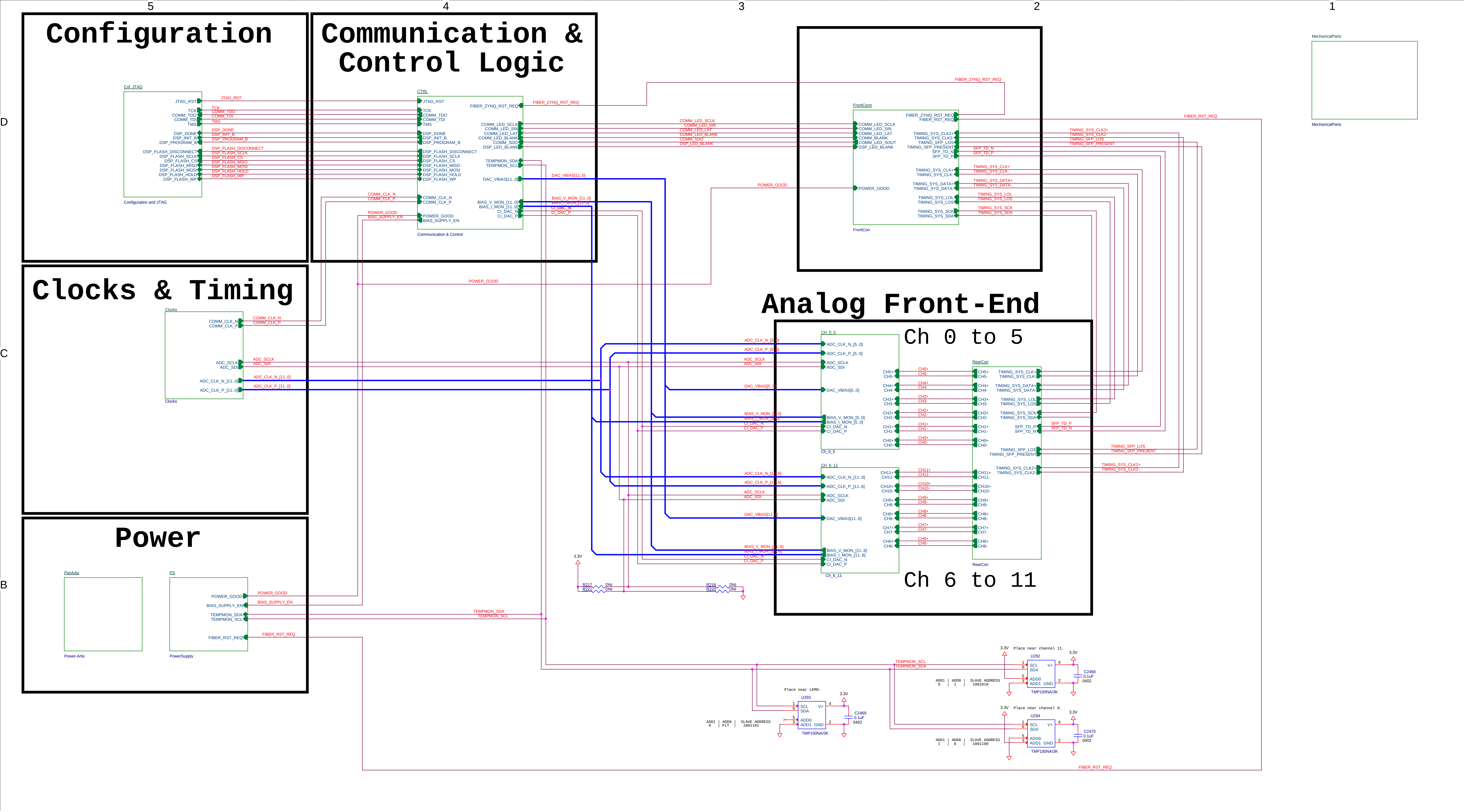

Configuration
Communication &
Control Logic
Clocks & Timing
Power
Analog Front-End
Ch 0 to 5
Ch 6 to 11
Cnf_JTAG
Configuration and JTAG
JTAG_RST
TCK
COMM_TDO
COMM_TDI
TMS
DSP_DONE
DSP_INIT_B
DSP_PROGRAM_B
DSP_FLASH_DISCONNECT
DSP_FLASH_SCLK
DSP_FLASH_CS
DSP_FLASH_MISO
DSP_FLASH_MOSI
DSP_FLASH_HOLD
DSP_FLASH_WP
CTRL
Communication & Control
FIBER_ZYNQ_RST_REQ
COMM_LED_SCLK
COMM_LED_SIN
COMM_LED_LAT
COMM_LED_BLANK
COMM_SDO
DSP_LED_BLANK
TEMPMON_SDA
TEMPMON_SCL
DAC_VBIAS[11..0]
COMM_CLK_N
COMM_CLK_P
BIAS_V_MON_[11..0]
BIAS_I_MON_[11..0]
CI_DAC_N
CI_DAC_P
POWER_GOOD
BIAS_SUPPLY_EN
FrontConn
FrontCon
FIBER_RST_REQ
COMM_BLANK
COMM_LED_SOUT
TIMING_SYS_CLK2+
TIMING_SYS_CLK2-
TIMING_SFP_LOS
TIMING_SFP_PRESENT
SFP_TD_N
SFP_TD_P
TIMING_SYS_CLK+
TIMING_SYS_CLK-
TIMING_SYS_DATA+
TIMING_SYS_DATA-
TIMING_SYS_LOL
TIMING_SYS_LOS
TIMING_SYS_SCK
TIMING_SYS_SDA
MechanicalParts
Clocks
ADC_SCLK
ADC_SDI
ADC_CLK_N_[11..0]
ADC_CLK_P_[11..0]
CH_0_5
Ch_0_5
ADC_CLK_N_[5..0]
ADC_CLK_P_[5..0]
DAC_VBIAS[5..0]
BIAS_V_MON_[5..0]
BIAS_I_MON_[5..0]
CH5+ CH5- CH4+ CH4- CH3+ CH3- CH2+ CH2- CH1+ CH1- CH0+ CH0-
CH_6_11
Ch_6_11
ADC_CLK_N_[11..6]
ADC_CLK_P_[11..6]
DAC_VBIAS[11..6]
BIAS_V_MON_[11..6]
BIAS_I_MON_[11..6]
CH11+ CH11- CH10+ CH10- CH9+ CH9- CH8+ CH8- CH7+ CH7- CH6+ CH6-
RearCon
PwrArtix
Power-Artix
PS
PowerSupply
3.3V
R217 DNI
R221 DNI
R216 DNI
R220 DNI
Place near LEMO.
U293
SCL SDA ADD0 ADD1 V+ GND
TMP100NA/3K
C2469 0.1uF 0402
ADD1 | ADD0 | SLAVE ADDRESS
0 | FLT | 1001101
Place near channel 11.
U292
C2468 0.1uF 0402
ADD1 | ADD0 | SLAVE ADDRESS
0 | 1 | 1001010
Place near channel 0.
U294
C2470 0.1uF 0402
ADD1 | ADD0 | SLAVE ADDRESS
1 | 0 | 1001100

DATE	BY	OLD FILE NAME	NEW FILE NAME
1-30-2017	JOHN ANDERSON	13PC041_RevA_AsBuilt	17PC001
10-28-2013	TIM CUNDIFF	13PC041_10_25_2013	13PC041_10_28_2013
10-25-2013	MIKE OBERLING	13PC041	13PC041_10_25_2013

Title: Top

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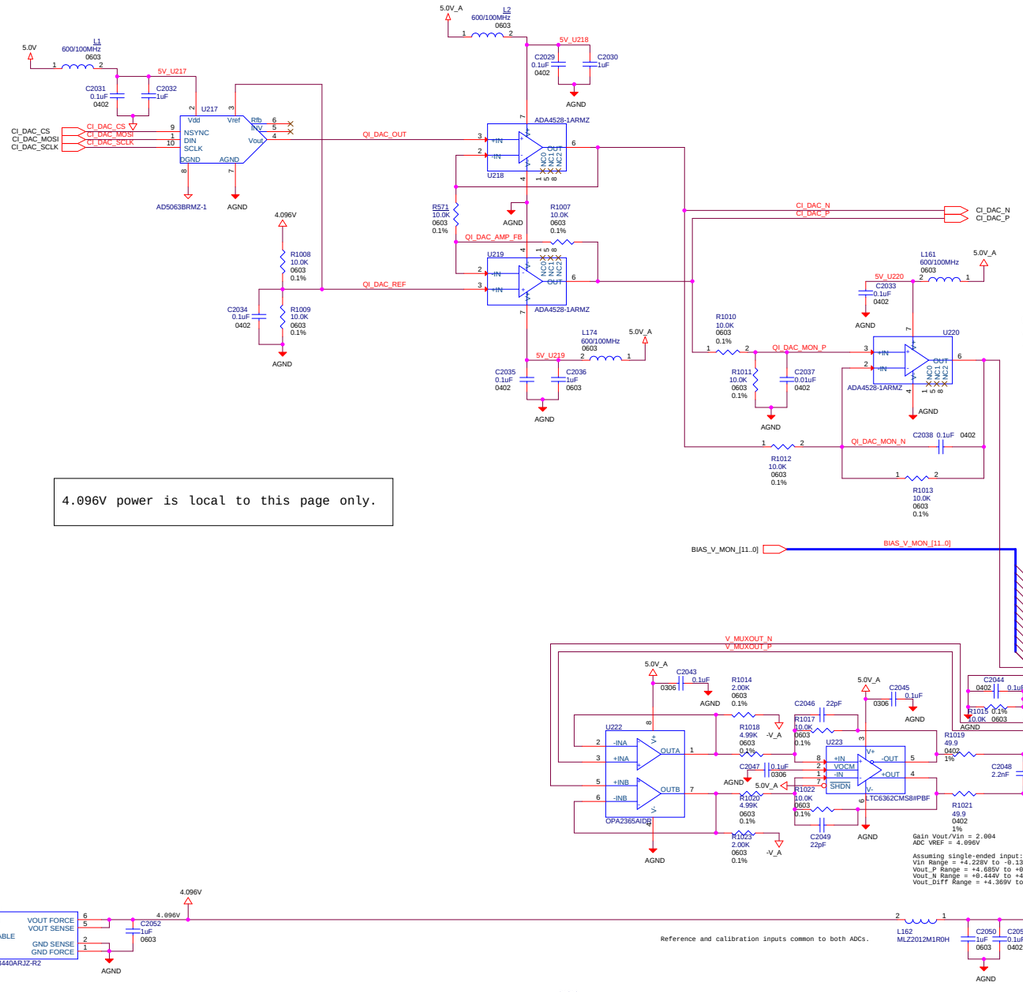
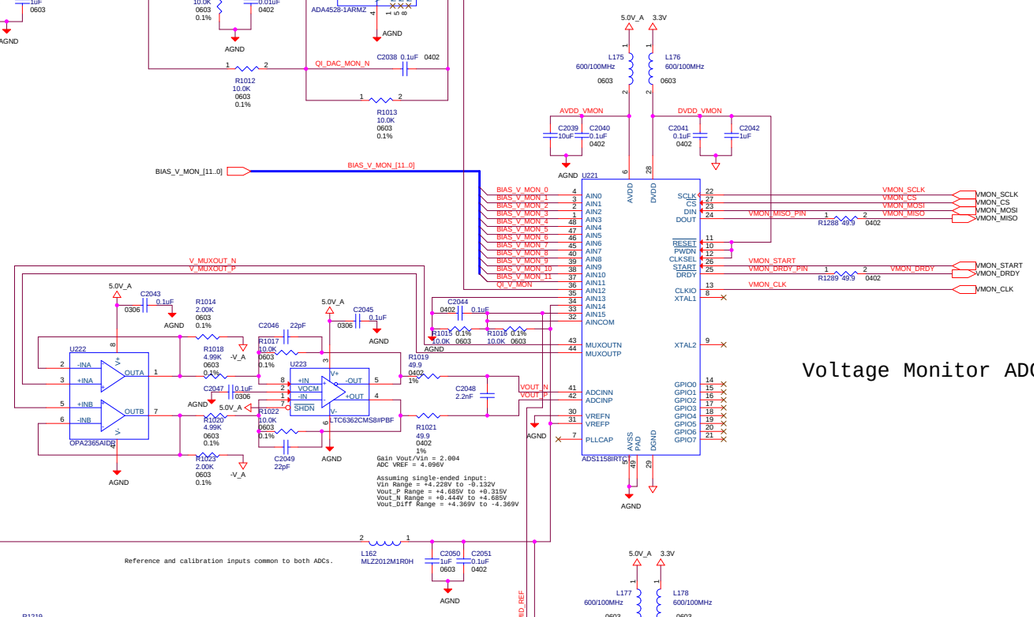
Charge Injection



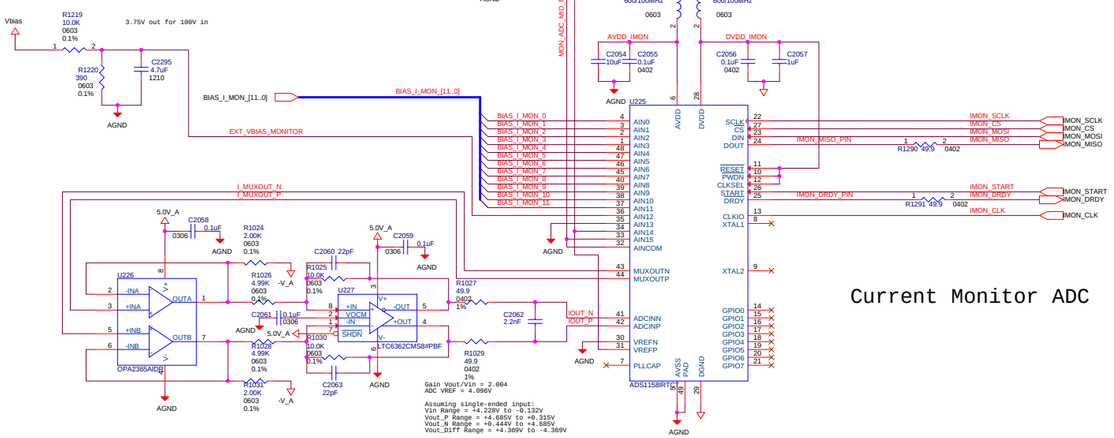
4.096V power is local to this page only.

Charge injection control voltage buffer for readback through Voltage Monitor

Voltage Monitor ADC



Reference and calibration inputs common to both ADCs.



Current Monitor ADC

Title: Analog			
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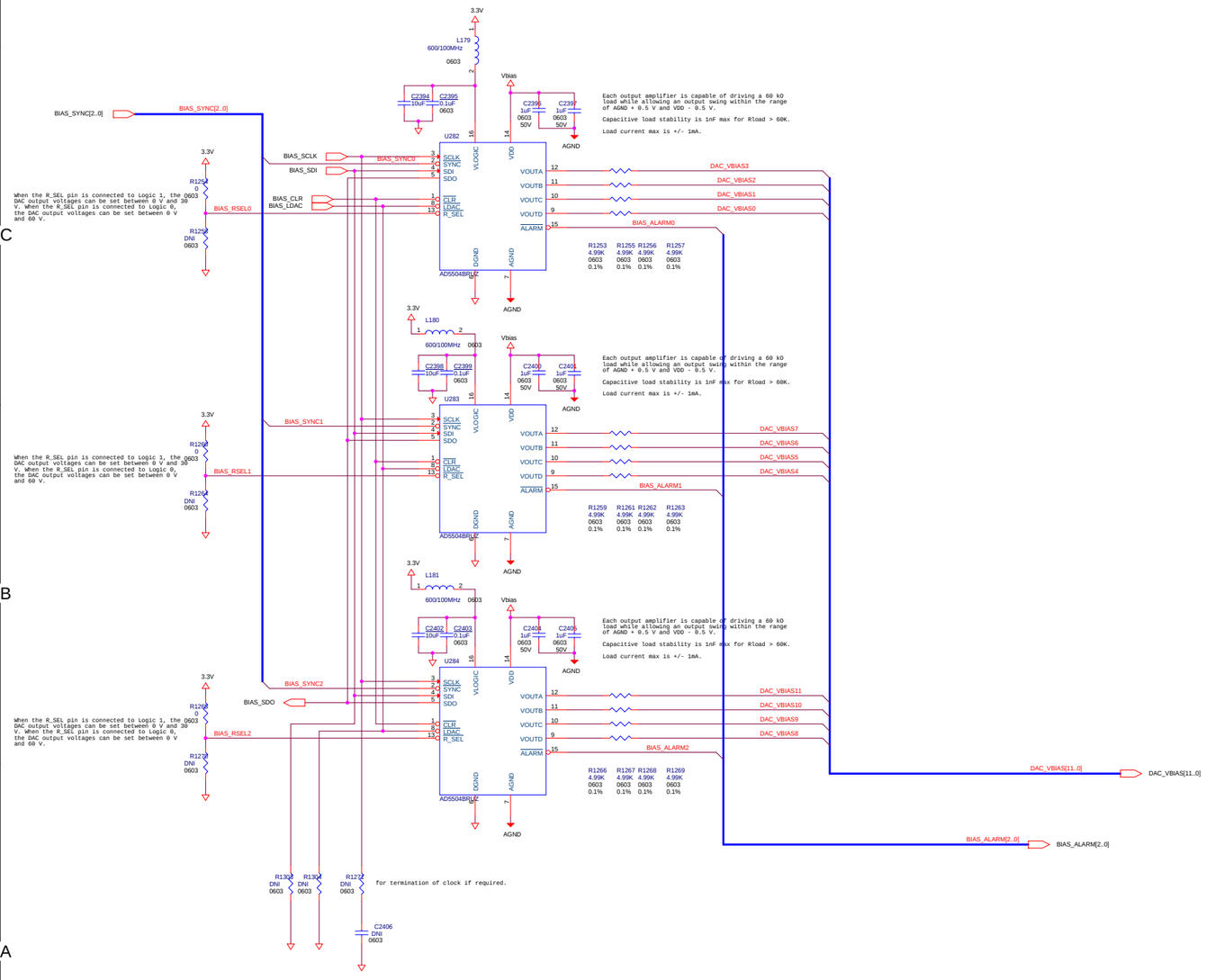

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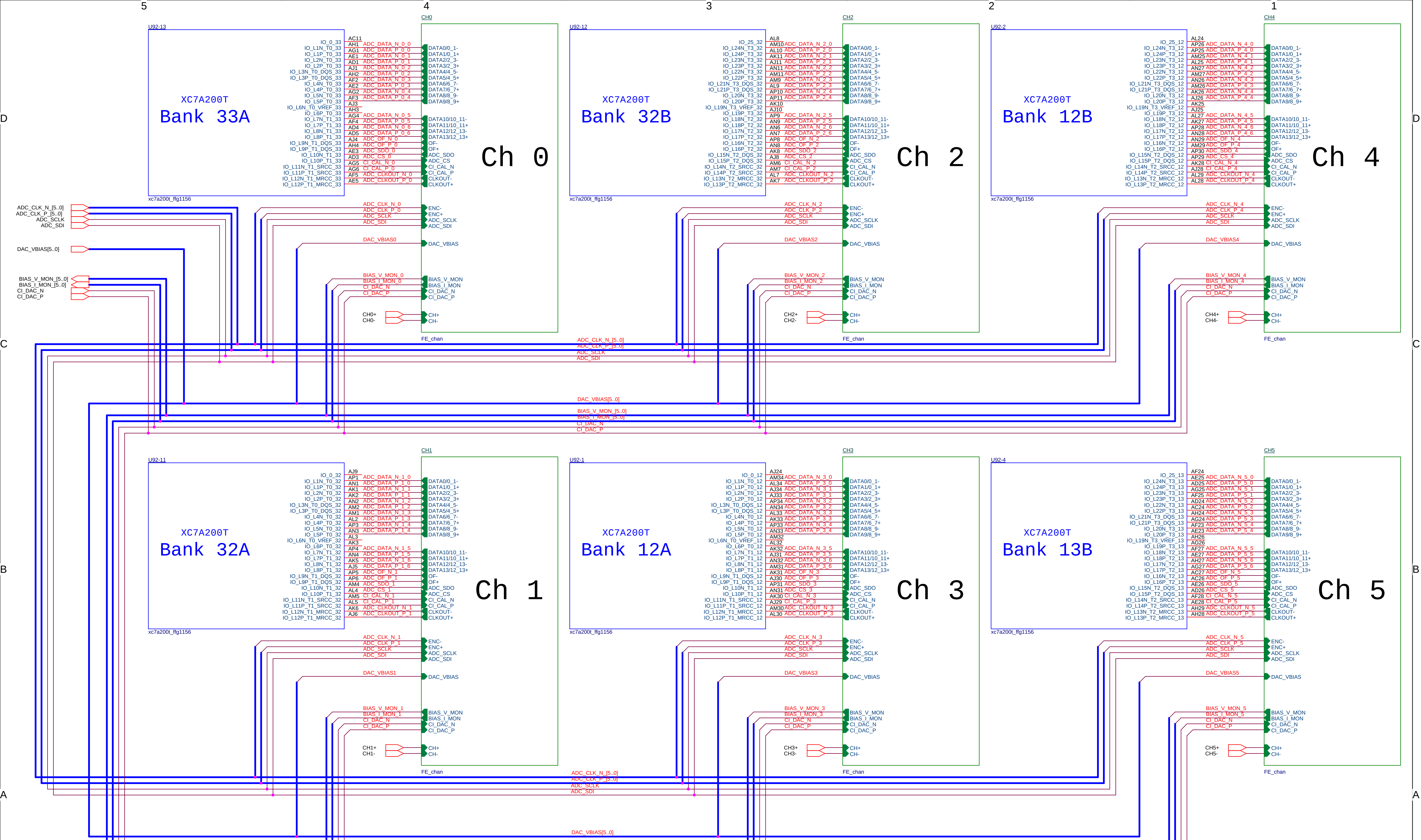

Title
Channel 0 to 5

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Custom	PC17001A	A

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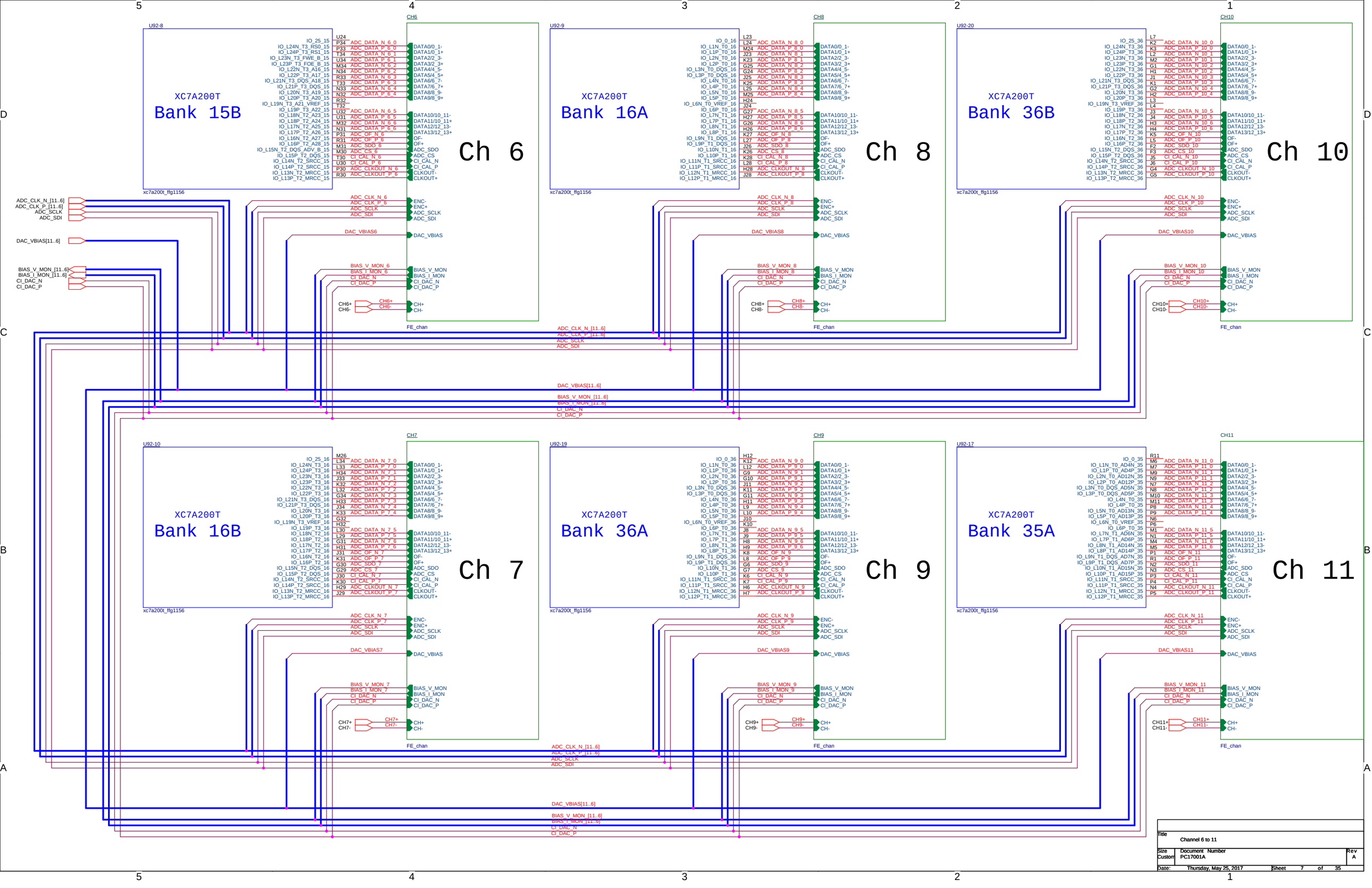
U92-8
XC7A200T
Bank 15B
xc7a200t_ffg1156
CH6
Ch 6
FE_chan
U92-9
XC7A200T
Bank 16A
xc7a200t_ffg1156
CH8
Ch 8
FE_chan
U92-20
XC7A200T
Bank 36B
xc7a200t_ffg1156
CH10
Ch 10
FE_chan
U92-10
XC7A200T
Bank 16B
xc7a200t_ffg1156
CH7
Ch 7
FE_chan
U92-19
XC7A200T
Bank 36A
xc7a200t_ffg1156
CH9
Ch 9
FE_chan
U92-17
XC7A200T
Bank 35A
xc7a200t_ffg1156
CH11
Ch 11
FE_chan
ADC_CLK_N_[11..6]
ADC_CLK_P_[11..6]
ADC_SCLK
ADC_SDI
DAC_VBIAS[11..6]
BIAS_V_MON_[11..6]
BIAS_I_MON_[11..6]
CI_DAC_N
CI_DAC_P
Title
Channel 6 to 11
Size
Custom
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A
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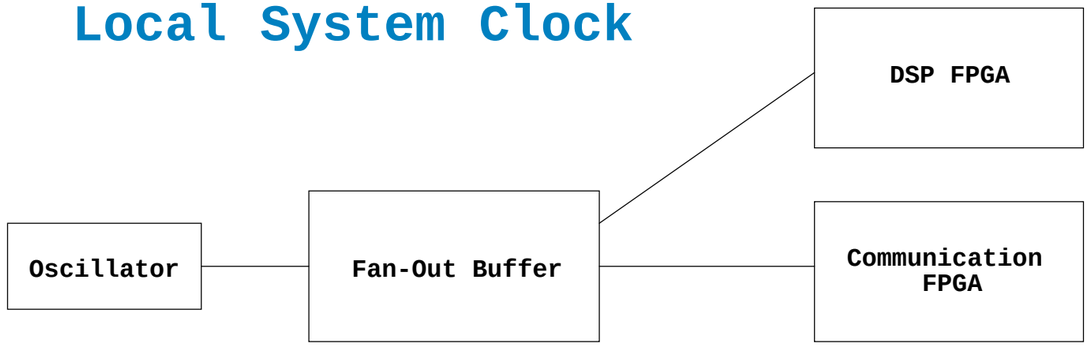
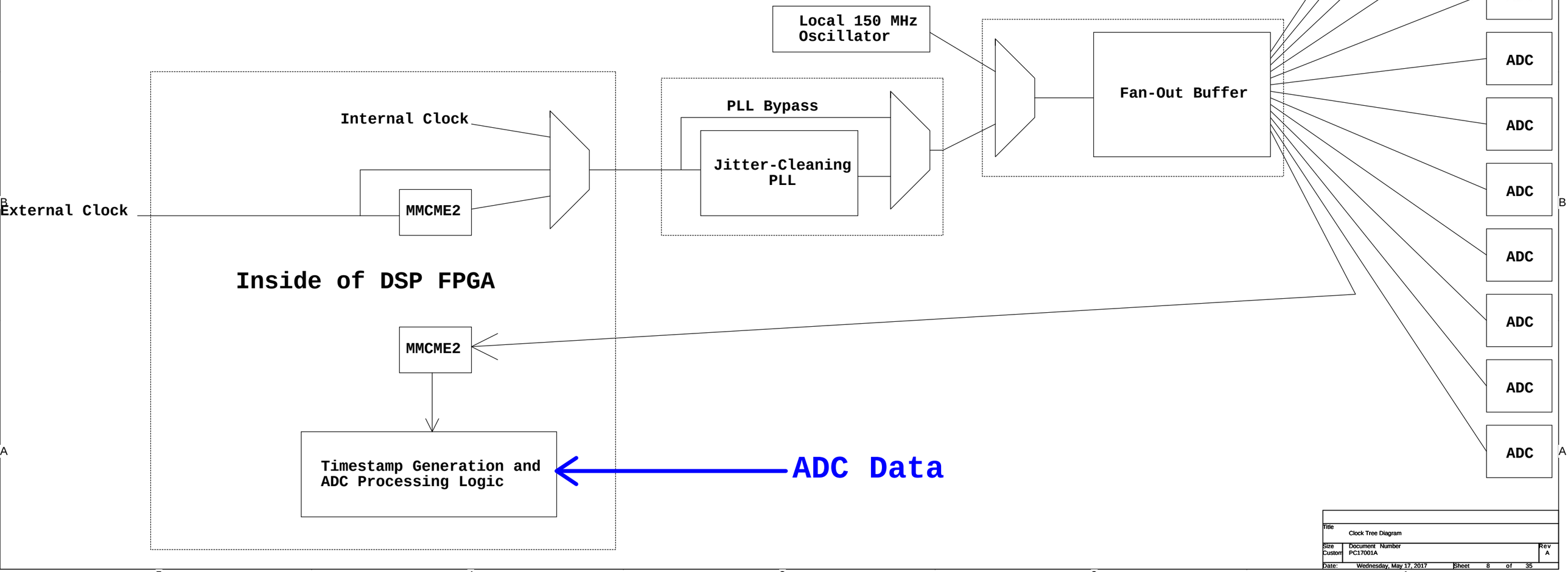
Local System Clock



ADC Clock



Title	Clock Tree Diagram	
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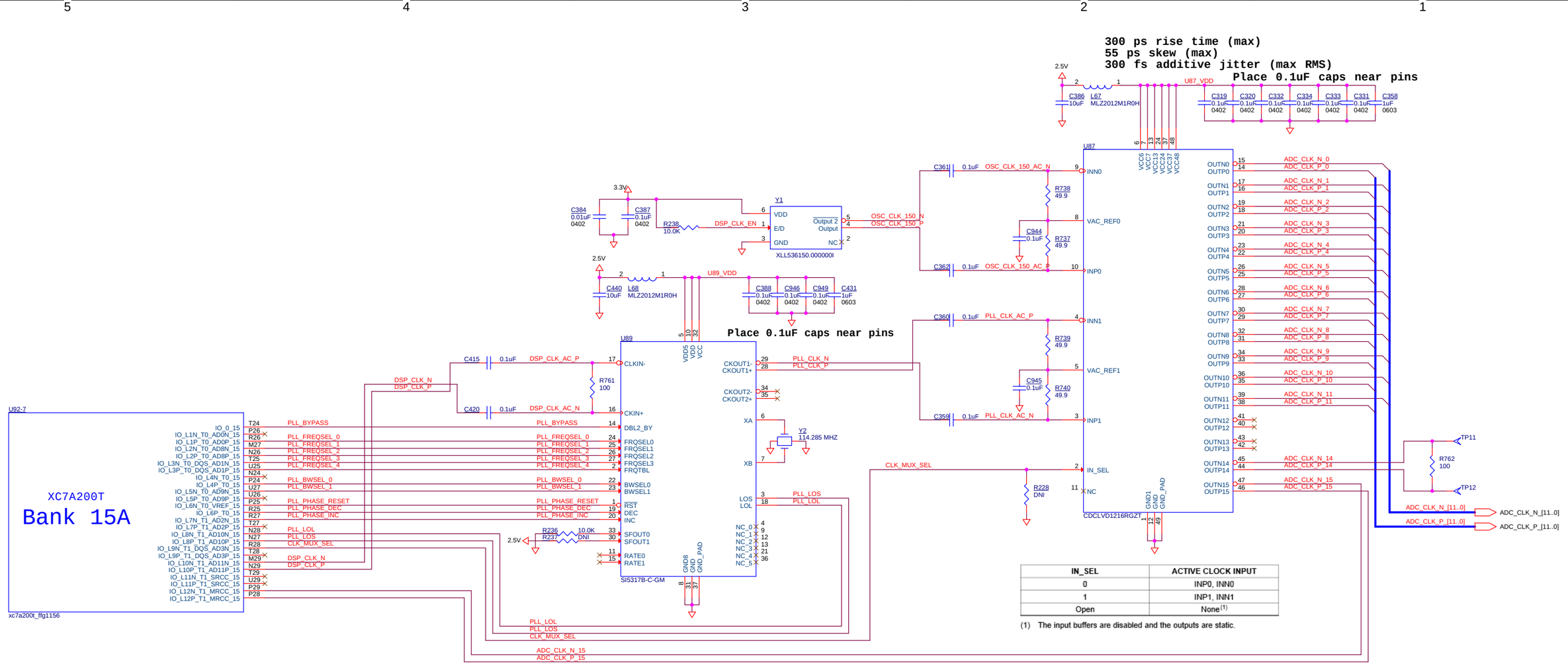
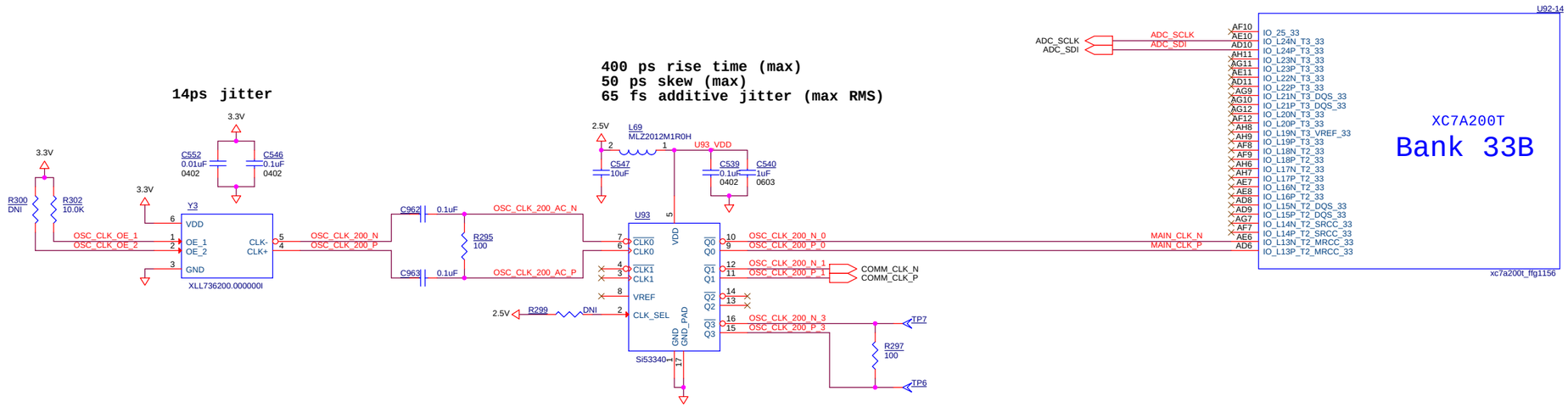

300 ps rise time (max)
55 ps skew (max)
300 fs additive jitter (max RMS)
Place 0.1uF caps near pins
U87_VDD
U87
U89_VDD
U89
Place 0.1uF caps near pins
U92-7
XC7A200T
Bank 15A
xc7a200t_ffg1156
SI5317B-C-GM
XLL536150.000000I
CDCLVD1216RGZT
Y1
Y2
114.285 MHZ
OSC_CLK_150_AC_N
OSC_CLK_150_AC_P
PLL_CLK_AC_P
PLL_CLK_AC_N
DSP_CLK_AC_P
DSP_CLK_AC_N
DSP_CLK_EN
PLL_CLK_N
PLL_CLK_P
PLL_LOS
CLK_MUX_SEL
ADC_CLK_N_[11..0]
ADC_CLK_P_[11..0]
IN_SEL
ACTIVE CLOCK INPUT
0
INP0, INN0
1
INP1, INN1
Open
None(1)
(1) The input buffers are disabled and the outputs are static.


14ps jitter
400 ps rise time (max)
50 ps skew (max)
65 fs additive jitter (max RMS)
U92-14
XC7A200T
Bank 33B
xc7a200t_ffg1156
XLL736200.000000I
Si53340-H
ADC_SCLK
ADC_SDI
MAIN_CLK_N
MAIN_CLK_P
COMM_CLK_N
COMM_CLK_P
OSC_CLK_200_AC_N
OSC_CLK_200_AC_P
OSC_CLK_OE_1
OSC_CLK_OE_2

333 MHz Data Rate
1.065 Gb/s

U92-15

XC7A200T
Bank 34A

xc7a200t_ffg1156

U92-16

XC7A200T
Bank 34B

xc7a200t_ffg1156

AXI Chip2Chip Bridge
50 MHz Data Rate

Zynq_Block

3 new differential pairs for interface expansion

JTAG

DSP Config

Voltage Monitor

Current Monitor

Charge Injection

Clock

DSP Flash Memory

BIAS Control

Status LEDs

Analog

Zynq_Block

Title	Communication & Control		
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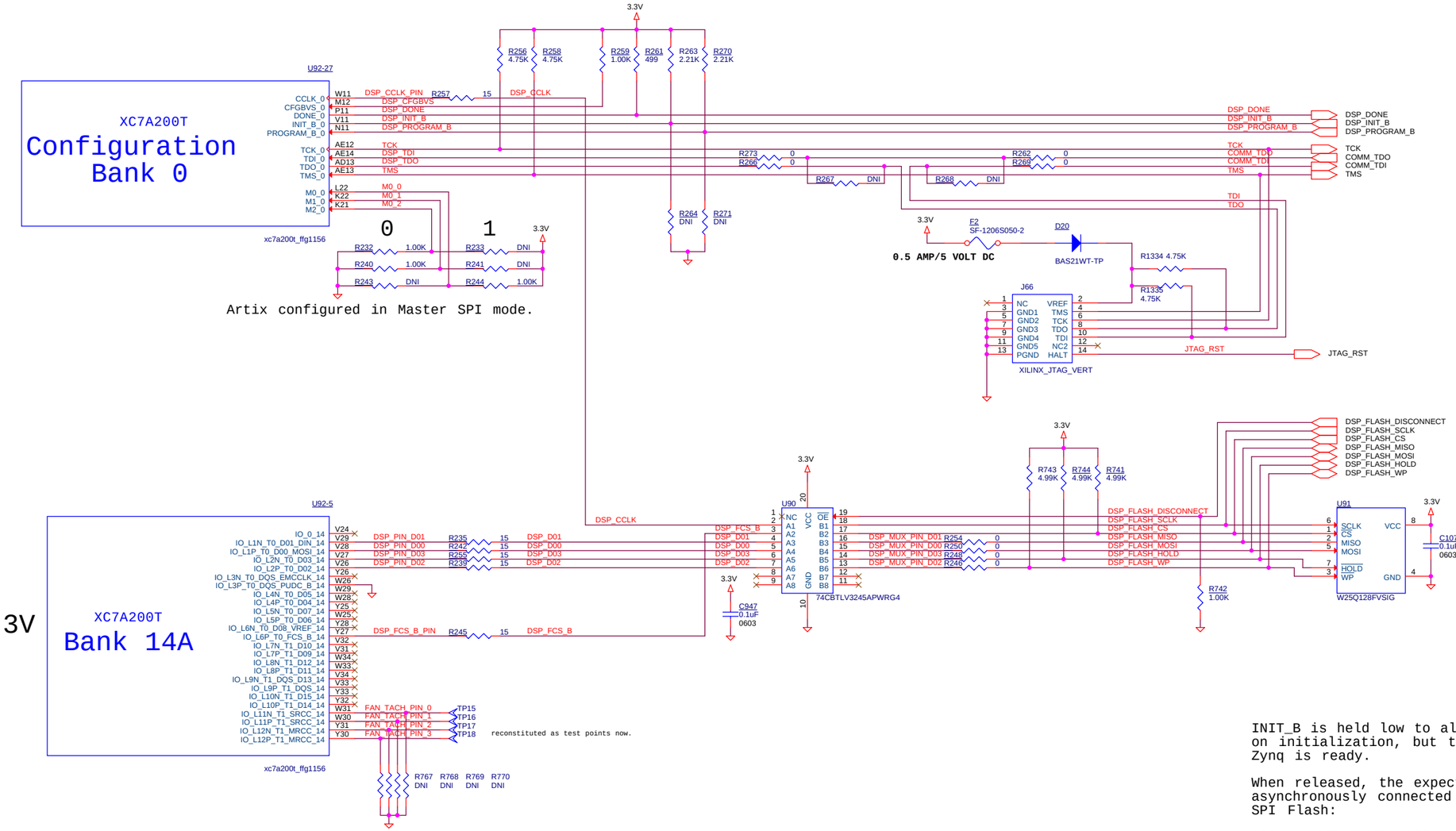

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	x1	Output
Master SPI	001	x1, x2, x4	Output
Master BPI	010	x8, x16	Output
Master SelectMAP	100	x8, x16	Output
JTAG	101	x1	Not Applicable
Slave SelectMAP	110	x8, x16, x32(1)	Input
Slave Serial(2)	111	x1	Input

INIT_B is held low to allow the FPGA to complete is power on initialization, but to hold off configuration until Zynq is ready.

When released, the expectation is that the Zynq has asynchronously connected the following signals to the SPI Flash:

D00 => DSP_FLASH_MOSI
D01 => DSP_FLASH_MISO
D02 => DSP_FLASH_WP
D03 => DSP_FLASH_HOLD
FCS_B => DSP_FLASH_CS
CCLK => DSP_FLASH_SCLK

From this point the Artix auto-magically configures itself, without further intervention from the SmartFusion.

The Zynq can re-assume control over the flash at any time by driving the PROGRAM_B line low, or the INIT_B line low. The difference being that PROGRAM_B will reinitialize the DSP FPGA, whereas INIT_B merely prevents it from configuring.

Flash may be programmed directly through JTAG, or via the Zynq

Max Throughput = 60 MHz x 4 Bits (QSPI) = 240 Mb/s
Config Time = 77,845,216 bits / (240 Mb/s) = 324 ms (approx.)

MAMS Motherboard			
Title: Configuration and JTAG			
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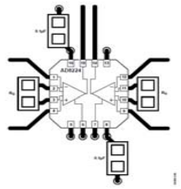
EXAMPLE LAYOUT OF AD8224



Vmon: gain of 1
Imon : gain of 4

Vmon output divided by 10 prior to ADC

Desired current monitor characteristics:
Range 0 - 200uA
Resolution 100nA

5K and gain of 4 does this nicely, but has problem if SiPM shorts out. Current is then 2mA and Vout jumps towards positive rail (Vbias), overdriving ADC.

If we put a 10:1 divider on output of current monitor, this moves the range to 0-2mA without overdriving the ADC, but cuts resolution to 2uV/nA. Assuming 14 bit ADC with input range of 4.096V, that's about 125nA/count.

Voltage measured after current shunt to include load of Vmon in current measurement, and to simplify calculation of SiPM applied voltage.

Series resistors provide 50k * 5pf low-pass (Fc = 600kHz) based on input characteristics given in data sheet.

EIA resistor values
16.0K 4.0875
16.2K 4.0494
16.5K 3.9939
16.9K 3.9231

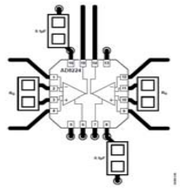
Rg = 49.4K/(G-1)
Gain of 4: 16.47K
Gain of 1: open

Charge injection path

Load for other side of op-amp to balance impedance of charge injection network

POSITIVE BIAS VOLTAGE
'-' SIGNAL OF RJ45 CONNECTOR
SiPM
'+' SIGNAL OF RJ45 CONNECTOR
BIAS RETURN THRU GND

EXAMPLE LAYOUT OF AD8224



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16.2K 4.0494
16.5K 3.9939
16.9K 3.9231

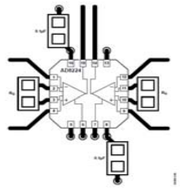
Rg = 49.4K/(G-1)
Gain of 4: 16.47K
Gain of 1: open

Charge injection path

Load for other side of op-amp to balance impedance of charge injection network

POSITIVE BIAS VOLTAGE
'-' SIGNAL OF RJ45 CONNECTOR
SiPM
'+' SIGNAL OF RJ45 CONNECTOR
BIAS RETURN THRU GND

EXAMPLE LAYOUT OF AD8224



Vmon: gain of 1
Imon : gain of 4

Vmon output divided by 10 prior to ADC

Desired current monitor characteristics:
Range 0 - 200uA
Resolution 100nA

5K and gain of 4 does this nicely, but has problem if SiPM shorts out. Current is then 2mA and Vout jumps towards positive rail (Vbias), overdriving ADC.

If we put a 10:1 divider on output of current monitor, this moves the range to 0-2mA without overdriving the ADC, but cuts resolution to 2uV/nA. Assuming 14 bit ADC with input range of 4.096V, that's about 125nA/count.

Voltage measured after current shunt to include load of Vmon in current measurement, and to simplify calculation of SiPM applied voltage.

Series resistors provide 50k * 5pf low-pass (Fc = 600khz) based on input characteristics given in data sheet.

EIA resistor values
16.0K 4.8875
16.2K 4.8494
16.5K 3.9939
16.9K 3.9231

Rg = 49.4K/(G-1)
Gain of 4: 16.47K
Gain of 1: open

Charge injection path

Load for other side of op-amp to balance impedance of charge injection network

POSITIVE BIAS VOLTAGE
'-' SIGNAL OF RJ45 CONNECTOR
SiPM
'+' SIGNAL OF RJ45 CONNECTOR
BIAS RETURN THRU GND

Title	Front-End Channel
Size D	Document Number PC17001A
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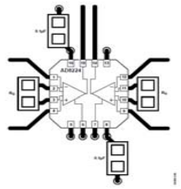
Date:	Thursday, May 25, 2017
Sheet	14 of 35

EXAMPLE LAYOUT OF AD8224



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Gain of 4: 16.47K
Gain of 1: open

EIA resistor values
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16.2K 4.8494
16.5K 3.9939
16.9K 3.9231

Charge injection path

Load for other side of op-amp to balance impedance of charge injection network

POSITIVE BIAS VOLTAGE
'-' SIGNAL OF RJ45 CONNECTOR
SiPM
'+' SIGNAL OF RJ45 CONNECTOR
BIAS RETURN THRU GND
CH+
CH-

Title: Front-End Channel
Size: D
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Rev: A
Date: Thursday, May 25, 2017
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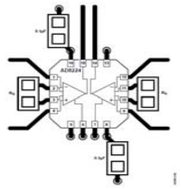
EXAMPLE LAYOUT OF AD8224



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Imon : gain of 4

Vmon output divided by 10 prior to ADC

Desired current monitor characteristics:
Range 0 - 200uA
Resolution 100nA

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Charge injection path

Load for other side of op-amp to balance impedance of charge injection network

POSITIVE BIAS VOLTAGE
'-' SIGNAL OF RJ45 CONNECTOR
SiPM
'+' SIGNAL OF RJ45 CONNECTOR
BIAS RETURN THRU GND

Title	Front-End Channel
Size: D	Document Number: PC17001A
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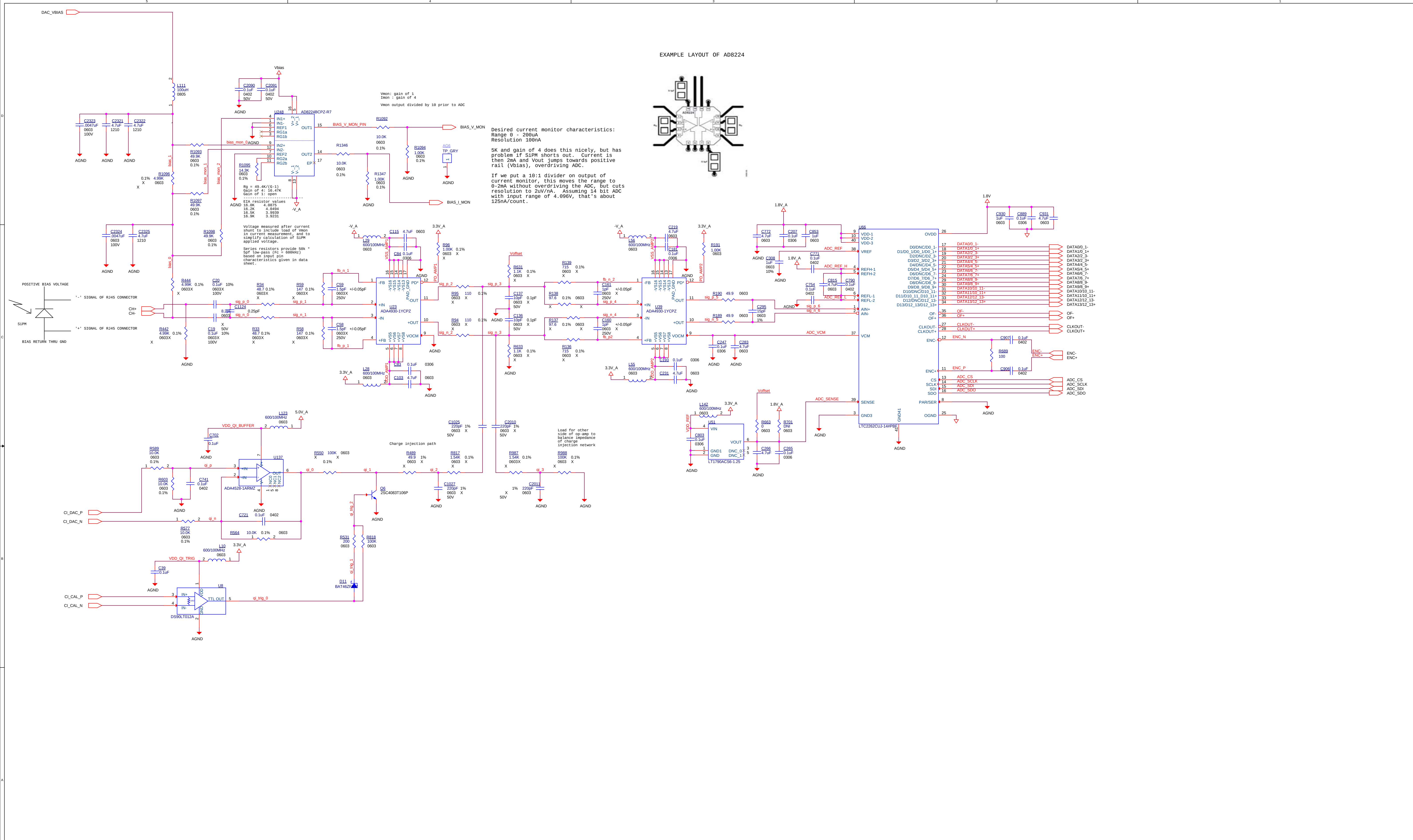
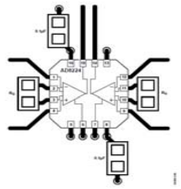
Date: Thursday, May 25, 2017	Sheet 16 of 35



Title	Front-End Channel		
Size D	Document Number PC17001A		Rev A
Date:	Thursday, May 25, 2017	Sheet 17	of 35

EXAMPLE LAYOUT OF AD8224



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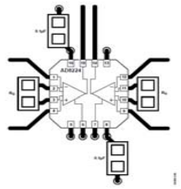
Charge injection path

Load for other side of op-amp to balance impedance of charge injection network

EXAMPLE LAYOUT OF AD8224



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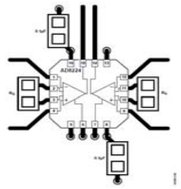
Charge injection path

Load for other side of op-amp to balance impedance of charge injection network

POSITIVE BIAS VOLTAGE
'-' SIGNAL OF RJ45 CONNECTOR
SiPM
'+' SIGNAL OF RJ45 CONNECTOR
BIAS RETURN THRU GND

EXAMPLE LAYOUT OF AD8224



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Charge injection path

Load for other side of op-amp to balance impedance of charge injection network

POSITIVE BIAS VOLTAGE
'-' SIGNAL OF RJ45 CONNECTOR
SiPM
'+' SIGNAL OF RJ45 CONNECTOR
BIAS RETURN THRU GND

Title	Front-End Channel
Size D	Document Number PC17001A
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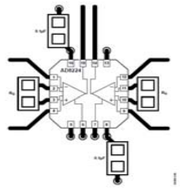
EXAMPLE LAYOUT OF AD8224



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Vmon output divided by 10 prior to ADC

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Charge injection path

Load for other side of op-amp to balance impedance of charge injection network

POSITIVE BIAS VOLTAGE
'-' SIGNAL OF RJ45 CONNECTOR
SiPM
'+' SIGNAL OF RJ45 CONNECTOR
BIAS RETURN THRU GND

Title	Front-End Channel
Size D	Document Number PC17001A
Rev	A
Date:	Thursday, May 25, 2017
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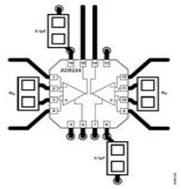
EXAMPLE LAYOUT OF AD8224



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Load for other side of op-amp to balance impedance of charge injection network

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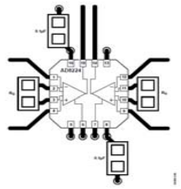

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Charge injection path

Load for other side of op-amp to balance impedance of charge injection network

POSITIVE BIAS VOLTAGE
'-' SIGNAL OF RJ45 CONNECTOR
SiPM
'+' SIGNAL OF RJ45 CONNECTOR
BIAS RETURN THRU GND

Used by Calibrator build only.

DIP #6) Implement correct 2nd jitter cleaner (removing Si5340, replace by Si5317). This is to allow for a separate jitter cleaning circuit dedicated to the timing interface.

400 ps rise time (max)
50 ps skew (max)
65 fs additive jitter (max RMS)

Optical output to trigger system.

Coax connector (vertical, inside box) for test output.

DIP #19) Consider hardware contolled power/bias LED.
DIP #20) Add voltage regulator and/or power monitor to generate two LED outputs : Bias Present and Bias OK. Bias Present should illuminate at as low a voltage as possible, Bias OK only when Vbias is within acceptable range (i.e. 34.0 – 34.2V).
DIP #22) As with DIP #20, there should also be Power Present and Power OK LEDs where PowerPresent means the Vicor is on and making 5V, Power OK means that in addition all Secondary voltages are within tolerance.

20170125: Cut out the TRIG and GPIO sections.

Left bank 35B untouched as this appears to be the hooks for the calibration module. Needs notes.

Signal from fiber optic receiver tied to MRCC pin of FPGA and thus can be used as GP input, trig input or clock.

Title	Front Panel Connection
Size: D	Document Number: PC17001A
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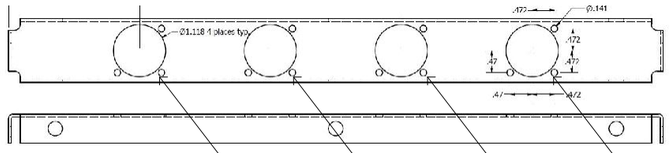
Date: Tuesday, June 06, 2017	Sheet 24 of 35



Bill of Materials Item
Left Side Panel
External to PC Board
BOM86
Proline
63-009-175-C
modified left side panel

Bill of Materials Item
Fan Screw
External to PC Board
BOM87

Bill of Materials Item
Fan Screw
External to PC Board
BOM88

Bill of Materials Item
Fan Screw
External to PC Board
BOM89

Bill of Materials Item
Fan Screw
External to PC Board
BOM90

Bill of Materials Item
Fan Screw
External to PC Board
BOM92

Bill of Materials Item
Fan Screw
External to PC Board
BOM93

Bill of Materials Item
Fan Screw
External to PC Board
BOM94

Bill of Materials Item
Fan Screw
External to PC Board
BOM95

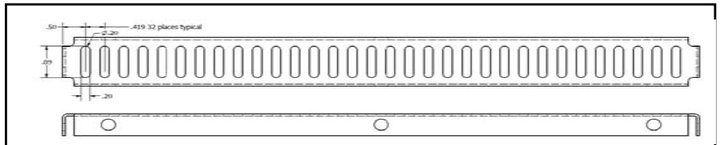
Bill of Materials Item
Fan Screw
External to PC Board
BOM96

Bill of Materials Item
Fan Screw
External to PC Board
BOM97

Bill of Materials Item
Fan Screw
External to PC Board
BOM98

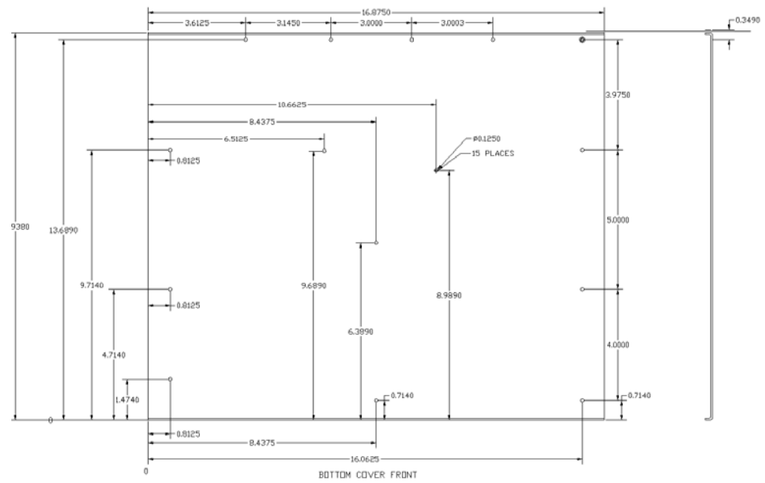
Bill of Materials Item
Fan Screw
External to PC Board
BOM99
McMaster
94779A410
fan screw 6-32 x 1/4 binder

Left side panel and screws for fans.
Fans called out on power supply page.



Bill of Materials Item
Right Side Panel
External to PC Board
BOM91
Proline
63-009-175-C
modified right side panel

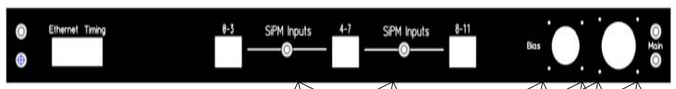
Right side panel



Bill of Materials Item
Bottom Cover Panel
External to PC Board
BOM100
Proline
64-006S-C
Modified Bottom panel

Bill of Materials Item
Top Cover Panel
External to PC Board
BOM101
Proline
64-006S-C
Top panel solid cover

Bottom Cover ***Top Cover***



Bill of Materials Item
Screw
External to PC Board
BOM102

Bill of Materials Item
Screw
External to PC Board
BOM103

Bill of Materials Item
L Bracket
External to PC Board
BOM104

Bill of Materials Item
Bias connector Screw
External to PC Board
BOM105

Bill of Materials Item
Main connector Screw
External to PC Board
BOM106

Bill of Materials Item
Screw
External to PC Board
BOM110

Bill of Materials Item
Screw
External to PC Board
BOM111

Bill of Materials Item
L Bracket
External to PC Board
BOM112
Allied
70181681
L Bracket 6-32

Bill of Materials Item
Bias connector Screw
External to PC Board
BOM113

Bill of Materials Item
Main connector Screw
External to PC Board
BOM114

Bill of Materials Item
Screw
External to PC Board
BOM117
McMaster
91253A146
Screw 6-32 x 3/8 flat head black

Bill of Materials Item
Screw
External to PC Board
BOM118
McMaster
91253A146
Screw 6-32 x 3/8 flat head black

Bill of Materials Item
Bias connector Screw
External to PC Board
BOM119

Bill of Materials Item
Main connector Screw
External to PC Board
BOM120

Bill of Materials Item
Bias connector Screw
External to PC Board
BOM121
McMaster
90283A108
Shield Screw 4-40 X 3/8 BINDER

Bill of Materials Item
Main connector Screw
External to PC Board
BOM122
McMaster
90283A108
Shield Screw 4-40 X 3/8 BINDER

Bill of Materials Item
Back Panel
External to PC Board
BOM123
Front Panel Express
Backpanel-17PC001A-A
Back Panel

Back Panel

Bill of Materials Item
Screw
External to PC Board
BOM107

Bill of Materials Item
Front Panel
External to PC Board
BOM108
Front Panel Express
Frontpanel-17PC001A-A
Front Panel

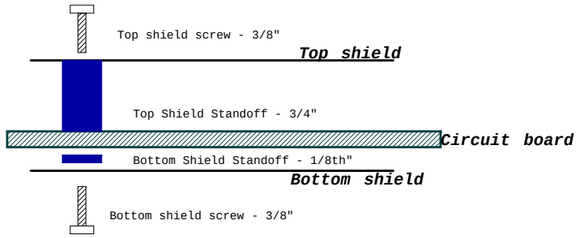
Bill of Materials Item
Screw
External to PC Board
BOM109

Bill of Materials Item
Screw
External to PC Board
BOM115
McMaster
91253A146
Screw 6-32 x 3/8 flat head black

Bill of Materials Item
Screw
External to PC Board
BOM116
McMaster
91253A146
Screw 6-32 x 3/8 flat head black

Front Panel

Title	<Title>	
Size D	Document Number <Doc>	Rev <RevCode>
Date: Friday, June 02, 2017	Sheet 25 of 35	



Bill of Materials Item
Bottom Shield Screw
External to PC Board
BOM6

Bill of Materials Item
Bottom Shield Standoff
External to PC Board
BOM7

Bill of Materials Item
Top Shield Standoff
External to PC Board
BOM5

Bill of Materials Item
Shield Top Screw
External to PC Board
BOM128

Bill of Materials Item
Bottom Shield Screw
External to PC Board
BOM9

Bill of Materials Item
Bottom Shield Standoff
External to PC Board
BOM10

Bill of Materials Item
Top Shield Standoff
External to PC Board
BOM8

Bill of Materials Item
Shield Top Screw
External to PC Board
BOM132

Bill of Materials Item
Bottom Shield Screw
External to PC Board
BOM12

Bill of Materials Item
Bottom Shield Standoff
External to PC Board
BOM13

Bill of Materials Item
Top Shield Standoff
External to PC Board
BOM11

Bill of Materials Item
Shield Top Screw
External to PC Board
BOM136

Bill of Materials Item
Bottom Shield Screw
External to PC Board
BOM15

Bill of Materials Item
Bottom Shield Standoff
External to PC Board
BOM16

Bill of Materials Item
Top Shield Standoff
External to PC Board
BOM14

Bill of Materials Item
Shield Top Screw
External to PC Board
BOM140

Bill of Materials Item
Bottom Shield Screw
External to PC Board
BOM18

Bill of Materials Item
Bottom Shield Standoff
External to PC Board
BOM19

Bill of Materials Item
Top Shield Standoff
External to PC Board
BOM17

Bill of Materials Item
Shield Top Screw
External to PC Board
BOM141

Bill of Materials Item
Bottom Shield Screw
External to PC Board
BOM21

Bill of Materials Item
Bottom Shield Standoff
External to PC Board
BOM22

Bill of Materials Item
Top Shield Standoff
External to PC Board
BOM20

Bill of Materials Item
Shield Top Screw
External to PC Board
BOM142

Bill of Materials Item
Bottom Shield Screw
External to PC Board
BOM24

Bill of Materials Item
Bottom Shield Standoff
External to PC Board
BOM25

Bill of Materials Item
Top Shield Standoff
External to PC Board
BOM23

Bill of Materials Item
Shield Top Screw
External to PC Board
BOM143

Bill of Materials Item
Bottom Shield Screw
External to PC Board
BOM27

Bill of Materials Item
Bottom Shield Standoff
External to PC Board
BOM28

Bill of Materials Item
Top Shield Standoff
External to PC Board
BOM26

Bill of Materials Item
Shield Top Screw
External to PC Board
BOM146

Bill of Materials Item
Bottom Shield Screw
External to PC Board
BOM30

Bill of Materials Item
Bottom Shield Standoff
External to PC Board
BOM31

Bill of Materials Item
Top Shield Standoff
External to PC Board
BOM29

Bill of Materials Item
Shield Top Screw
External to PC Board
BOM147

Bill of Materials Item
Bottom Shield Screw
External to PC Board
BOM33

Bill of Materials Item
Bottom Shield Standoff
External to PC Board
BOM34

Bill of Materials Item
Top Shield Standoff
External to PC Board
BOM32

Bill of Materials Item
Shield Top Screw
External to PC Board
BOM148

Bill of Materials Item
Bottom Shield Screw
External to PC Board
BOM36

Bill of Materials Item
Bottom Shield Standoff
External to PC Board
BOM37

Bill of Materials Item
Top Shield Standoff
External to PC Board
BOM35

Bill of Materials Item
Shield Top Screw
External to PC Board
BOM149

Bill of Materials Item
Bottom Shield Screw
External to PC Board
BOM39
McMaster
90283A108
Shield Screw 4-40 X 3/8 BINDER

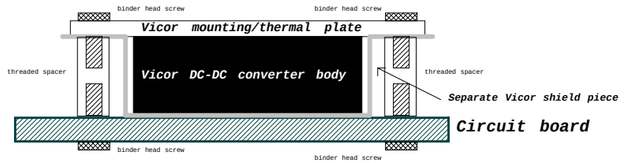
Bill of Materials Item
Bottom Shield Standoff
External to PC Board
BOM40
McMaster
91115A160
Shield Spacer 4-40 X 1/8 THRD

Bill of Materials Item
Top Shield Standoff
External to PC Board
BOM38
McMaster
91115A166
Shield Standoff 4-40 X 3/4 THRD

Bill of Materials Item
Shield Top Screw
External to PC Board
BOM150
McMaster
90283A108
Shield Screw 4-40 X 3/8 BINDER

Mounting Parts for Shield Plates

Shield has 12 mounting holes



Top screws

Bottom screws

Bill of Materials Item
Vicor Shield
External to PC Board
BOM124
Vicor shield (5/pack)
Digi-Key
1102-1634

Bill of Materials Item
Vicor Standoff
External to PC Board
BOM125

Bill of Materials Item
Vicor Shield Screw
External to PC Board
BOM126

Bill of Materials Item
Vicor Shield Screw
External to PC Board
BOM127

Bill of Materials Item
Vicor Standoff
External to PC Board
BOM129

Bill of Materials Item
Vicor Shield Screw
External to PC Board
BOM130

Bill of Materials Item
Vicor Shield Screw
External to PC Board
BOM131

Bill of Materials Item
Vicor Standoff
External to PC Board
BOM133

Bill of Materials Item
Vicor Shield Screw
External to PC Board
BOM134

Bill of Materials Item
Vicor Shield Screw
External to PC Board
BOM135

Bill of Materials Item
Vicor Standoff
External to PC Board
BOM137
McMaster
91115A163
VICOR 4-40 x 3/8 standoff thrd

Bill of Materials Item
Vicor Shield Screw
External to PC Board
BOM138
McMaster
90283A108
Shield Screw 4-40 X 3/8 BINDER

Bill of Materials Item
Vicor Shield Screw
External to PC Board
BOM139
McMaster
90283A108
Shield Screw 4-40 X 3/8 BINDER

Mounting Parts for Vicor DC-DC converter (U255)

Bill of Materials Item
FPGA Heatsink
External to PC Board
BOM144
Arrow
3718248000034G
FPGA Heatsink

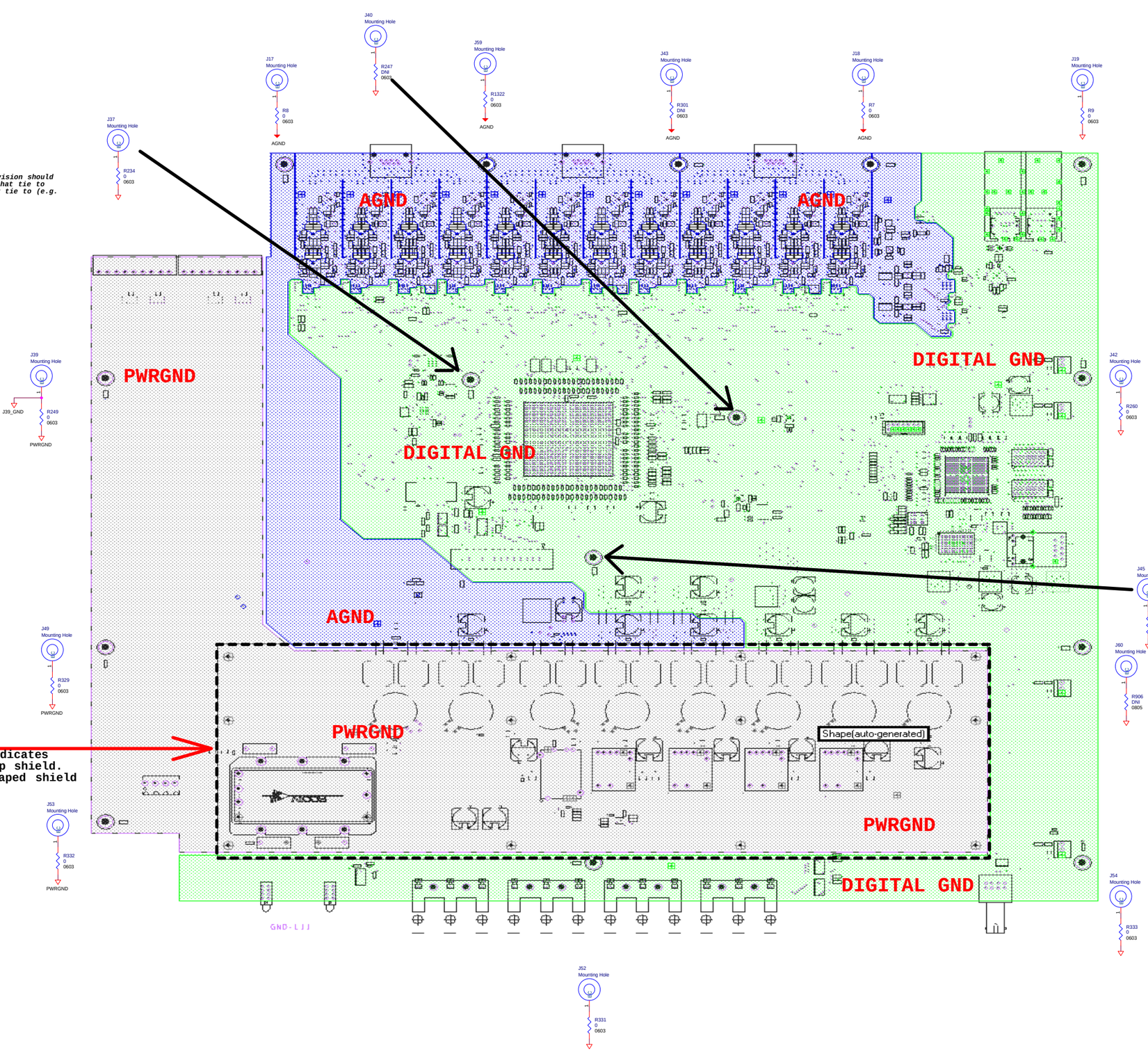
Bill of Materials Item
UZ1 heatsink
External to PC Board
BOM145
Digi-Key
ATS1264-ND
UZ1 Heatsink

Heat sinks added to FPGA's after assembly

Title	<Title>		
Size D	Document Number <Doc>		Rev <RevCode>
Date: Friday, June 02, 2017	Sheet 26 of 35		

This page describes all mechanical connections between the PC board and the chassis.

DIP #10) Silkscreen for next revision should explicitly label all resistors that tie to standoffs by which "ground" they tie to (e.g. DGND, AGND, PWRGND).

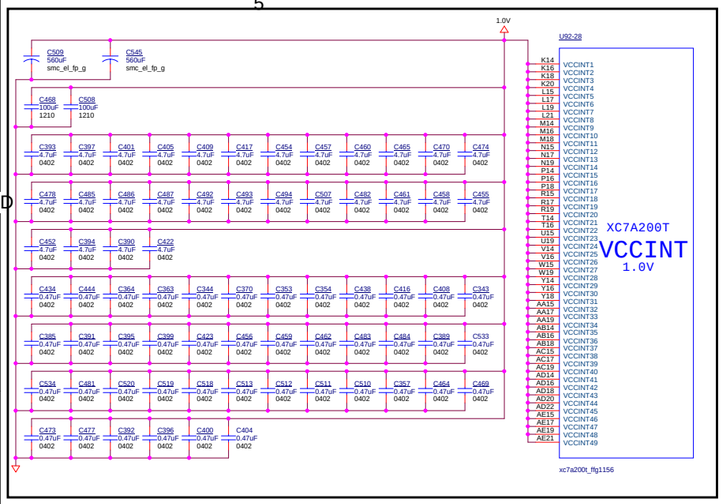


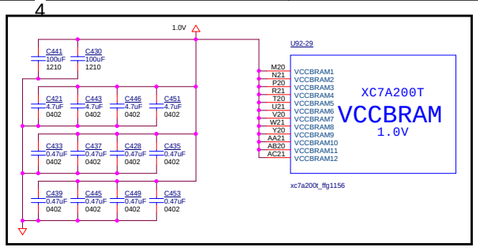
Dashed line indicates position of top shield. Identically shaped shield on bottom.

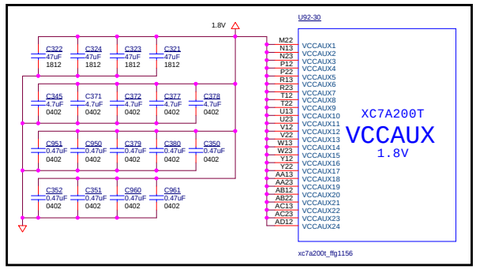
J19	Bill of Materials Item Board Standoff External to PC Board BOM41	Bill of Materials Item Board Top Screw External to PC Board BOM42	Bill of Materials Item Bottom Plate Screw External to PC Board BOM43
J18	Bill of Materials Item Board Standoff External to PC Board BOM44	Bill of Materials Item Board Top Screw External to PC Board BOM45	Bill of Materials Item Bottom Plate Screw External to PC Board BOM46
J43	Bill of Materials Item Board Standoff External to PC Board BOM47	Bill of Materials Item Board Top Screw External to PC Board BOM48	Bill of Materials Item Bottom Plate Screw External to PC Board BOM49
J59	Bill of Materials Item Board Standoff External to PC Board BOM50	Bill of Materials Item Board Top Screw External to PC Board BOM51	Bill of Materials Item Bottom Plate Screw External to PC Board BOM52
J17	Bill of Materials Item Board Standoff External to PC Board BOM53	Bill of Materials Item Board Top Screw External to PC Board BOM54	Bill of Materials Item Bottom Plate Screw External to PC Board BOM55
J39	Bill of Materials Item Board Standoff External to PC Board BOM56	Bill of Materials Item Board Top Screw External to PC Board BOM57	Bill of Materials Item Bottom Plate Screw External to PC Board BOM58
J49	Bill of Materials Item Board Standoff External to PC Board BOM59	Bill of Materials Item Board Top Screw External to PC Board BOM60	Bill of Materials Item Bottom Plate Screw External to PC Board BOM61
J53	Bill of Materials Item Board Standoff External to PC Board BOM62	Bill of Materials Item Board Top Screw External to PC Board BOM63	Bill of Materials Item Bottom Plate Screw External to PC Board BOM64
J52	Bill of Materials Item Board Standoff External to PC Board BOM65	Bill of Materials Item Board Top Screw External to PC Board BOM66	Bill of Materials Item Bottom Plate Screw External to PC Board BOM67
J54	Bill of Materials Item Board Standoff External to PC Board BOM68	Bill of Materials Item Board Top Screw External to PC Board BOM69	Bill of Materials Item Bottom Plate Screw External to PC Board BOM70
J60	Bill of Materials Item Board Standoff External to PC Board BOM71	Bill of Materials Item Board Top Screw External to PC Board BOM72	Bill of Materials Item Bottom Plate Screw External to PC Board BOM73
J42	Bill of Materials Item Board Standoff External to PC Board BOM74	Bill of Materials Item Board Top Screw External to PC Board BOM75	Bill of Materials Item Bottom Plate Screw External to PC Board BOM76
J45	Bill of Materials Item Board Standoff External to PC Board BOM77	Bill of Materials Item Board Top Screw External to PC Board BOM78	Bill of Materials Item Bottom Plate Screw External to PC Board BOM79
J40	Bill of Materials Item Board Standoff External to PC Board BOM80	Bill of Materials Item Board Top Screw External to PC Board BOM81	Bill of Materials Item Bottom Plate Screw External to PC Board BOM82
J37	Bill of Materials Item Board Standoff External to PC Board BOM83 McMaster 91115A162 Board Standoff 4-40 X 1/4 THRD	Bill of Materials Item Board Top Screw External to PC Board BOM84 McMaster 90283A105 Board Top Screw 4-40 X 3/16 BINDER	Bill of Materials Item Bottom Plate Screw External to PC Board BOM85 McMaster 90283A108 Shield Screw 4-40 X 3/8 BINDER

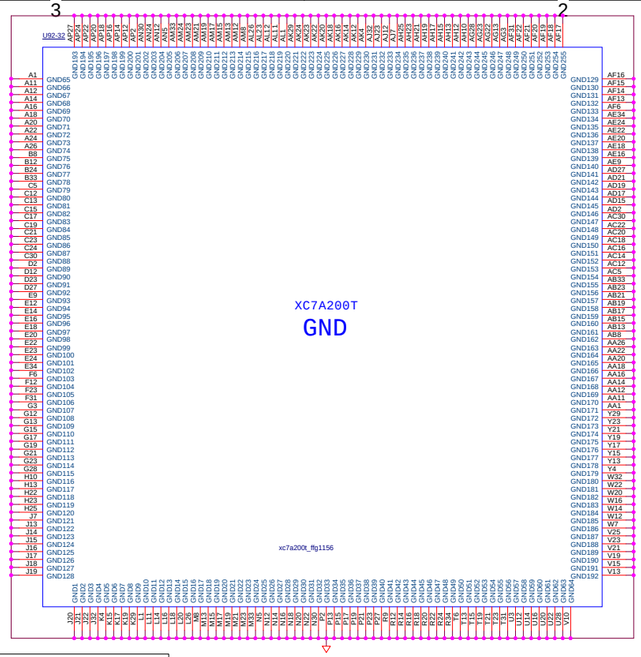
Screws, standoffs, etc. needed to mount PC board to chassis box. Does not include any mechanical items specific to the PC board (shields, heat sinks, etc.)

Title	PCB to chassis mechanics		
Size D	Document Number PC17001A		Rev A
Date:	Thursday, May 25, 2017	Sheet 27 of 35	









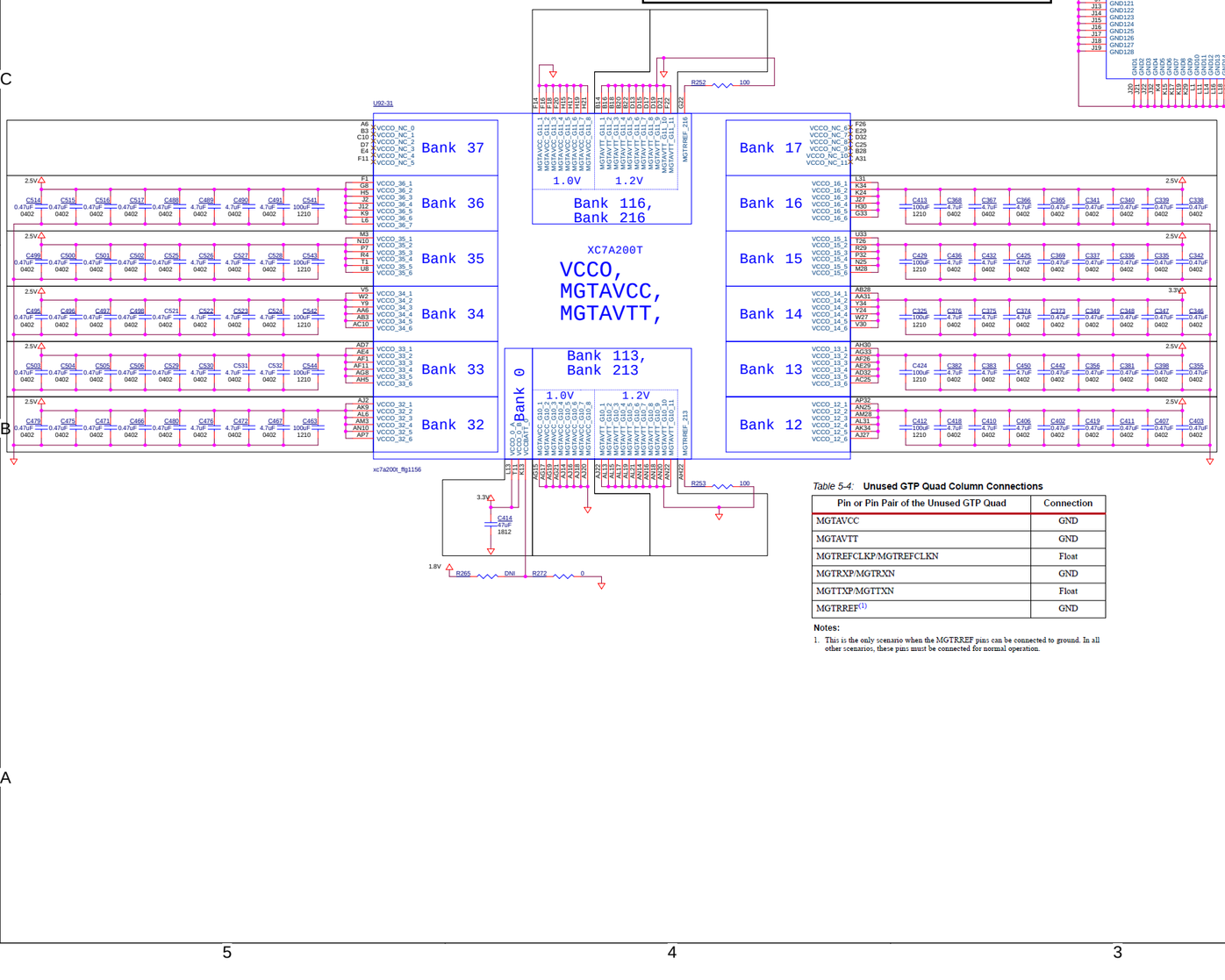


Table 5-4: **Unused GTP Quad Column Connections**

Pin or Pin Pair of the Unused GTP Quad	Connection
MGTAVCC	GND
MGTAVTT	GND
MGTREFCLKP/MGTREFCLKN	Float
MGTRXP/MGTRXN	GND
MGTTXP/MGTTXN	Float
MGTRREF[(1)]	GND

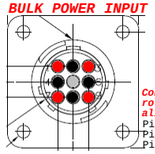
Notes:

1. This is the only scenario when the MGTRREF pins can be connected to ground. In all other scenarios, these pins must be connected for normal operation.

Title: Power-Artix LBNE Digitizer			
Size: D	Document Number: PC17001A		Rev: A
Date: Thursday, May 25, 2017	Sheet 28 of 35		

Main power and bias voltage to SSP is provided by external DC power supply through chassis mounted connectors using wire harnesses as sketched here.

BULK POWER INPUT



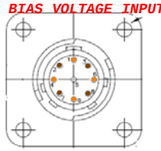
Pin 1
Pin 3
Pin 7
Pin 9
Pin 2
Pin 4
Pin 6
Pin 8
Pin 5

Connector is mounted to chassis in rotation as shown with large alignment lug UP.

Pins 1,3,7,9 are bulk power (V+)
Pins 2,4,6,8 are bulk power return (V-)
Pin 5 (center) is shield (chassis ground thru resistor)

Tyco 206705-1

BIAS VOLTAGE INPUT



Pin 1
Pin 4
Pin 6
Pin 9
Pin 2
Pin 7
Pin 8
Pin 3
Pin 5

Tyco 206486-1

Pins 1,2 are V+/V-
Pins 4,7 are V+/V-
Pins 9,8 are V+/V-
Pins 6,3 are V+/V-
Pin 5 (center) is shield (chassis ground thru resistor)

Connector is mounted to chassis in rotation as shown with large alignment lug UP.

FUSES FOR FUSE CLIPS ABOVE

Bill of Materials Item
2.25A
External to PC Board
F_PWR1

Bill of Materials Item
2.25A
External to PC Board
F_PWR2

Bill of Materials Item
500mA
External to PC Board
F_BIAS1

Bill of Materials Item
500mA
External to PC Board
F_BIAS2

J79 CON9 — BULK_POWER_V+ / BULK_POWER_V- / BULK_POWER_SHIELD — BK-6003 — FS3 BK-6003 R1329 DNI — FS4 BK-6003 — FUSED_POWER_V+ — VTP10 TP_BRN — PWRGND — PG3 TP_GRN — SW1 8GA2016-Z — R1330 DNI — J39_GND

J81 CON9 — EXTERNAL_BIAS_V+ / EXTERNAL_BIAS_V- / EXTERNAL_BIAS_SHIELD — FS5 BK-6003 — FS6 BK-6003 — FUSED_BIAS_V+ — FS7 BK-6003 R1331 DNI — FS8 BK-6003 — VTP11 TP_BRN — PWRGND — PG4 TP_GRN — R1332 DNI — J39_GND

Bat DOWN — Bat UP

SWITCHED_POWER_V+ — C2358 0.1uF 0402 50V — C2356 4.7uF 1210 — C2357 4.7uF 1210 — C2118 4700pF 1000V PWRGND — C2119 4700pF 1000V — U255 V28C5C50BL (+IN +OUT, PC SC, PR -OUT, -IN, PL1 PL2 PL3 PL4 PL5 PL6) — VICOR_PLATE — C2120 4700pF 1000V — C2121 4700pF 1000V — cappoly13_5x5_1x10_2ls — R1221 0 0603 — PWRGND

PLT pins are mounting plate holes for standoffs. Tie case to local fill area underneath converter to allow for grounding of baseplate.

Temperature monitor for U255 3.3V — U295 SCL SDA V+ ADD0 ADD1 GND — TMP100NA/3K — C2471 0.1uF 0402 — TEMPMON_SCL TEMPMON_SDA — ADD1 | ADD0 | SLAVE ADDRESS 0 | 0 | 1001000

SWITCHED_BIAS_V+ — C2359 0.047uF 0603 100V — C2360 4.7uF 1210 — C2361 4.7uF 1210 — L168 — PM3700-10-RC — L166 10uH mss1210 — L167 100 ohms 100 MHz SML-DM3312 — L169 10uH mss1210 — L170 100 ohms 100 MHz SML-DM3312 — C2362 0.047uF 0603 100V — C2363 4.7uF 1210 — C2364 4.7uF 1210 — AGND

5V–PreFilter — C603 0.1uF 0402 — C601 22uF 1210 — C615 560uF smc_el_fp_g — C614 560uF smc_el_fp_g — L100 — PM3700-10-RC — L89 10uH mss1210 — L77 DNI SML-DM3312 — L88 10uH mss1210 — L76 100 ohms 100 MHz SML-DM3312 — C587 0.1uF 0402 — C593 22uF 1210 — C581 560uF smc_el_fp_g — 5.0V_A — AGND

5V–PreFilter — C602 0.1uF 0402 — C608 22uF 1210 — C613 560uF SMC_EL_FP_G — L105 — PM3700-10-RC — L99 10uH mss1210 — L87 DNI SML-DM3312 — L98 10uH mss1210 — L86 100 ohms 100 MHz SML-DM3312 — C592 0.1uF 0402 — C598 22uF 1210 — C586 560uF SMC_EL_FP_G — 5.0V

+5V_A (analog) and +5V (digital) are developed in parallel as opposed to the other voltages in which the digital version is derived through a series filter from the analog.

Bill of Materials Item
100 ohms 100 MHz
External to PC Board
X L77

Bill of Materials Item
100 ohms 100 MHz
External to PC Board
X L87

Vout = 1.270V * (1 +R328/R327)
Want 36 - (-V_A), or about 34.2V to give current monitor maximum headroom.

226K gives 30.09
258K gives 34.17
255K gives 33.78

Vbias — U102 IN OUT SENSE/ADJ NC_#3 NC_#2 SHDN NC_#1 GND GND — LT3010EMSE#PBF — R328 255K 0603 — R327 10.0K 0603 — C580 1uF 0603 50V — AGND — Vbias_EXT — BIAS_SUPPLY_EN — R229 2.21K

DIP #3) Add test points for +1.4V post-filter and +1.8V_A. Explicitly define which inductors are DNI at assembly to disconnect rest of board from power supply outputs; include inductors as BOM ITEMs as inductors are added by ANL staff after power supplies are verified.

Rset = (10K * (0.69/(Vo-0.69))) - 1.43K

Original value of 17.4K yields 1.05V nominal
Change to 9.1K yields 1.345V
change to 8.3K for 1.4V

Bill of Materials Item
100 ohms 100 MHz
External to PC Board
X L83

Bill of Materials Item
100 ohms 100 MHz
External to PC Board
X L157

VTP21 TP_WHT

5V–PreFilter — R956 49.9 0402 — R957 DNI 0603 — U107 TPS3808G50DBVR (VCC SENSE, CT RESET, MR GND) — C1099 1000pF 0603 — C622 0.1uF 0402 — C616 DNI 0603 — PWRGND

FIBER_RST_REQ — internally pulled to +5 pre-filter thru 90K

5V–PreFilter — C1094 22uF 1210 — C1095 0.1uF 0402 — SYNC1 — U157 PTH04T260WAD (TRACK TT, VIN +SENSE, SYNC VOUT, INH/UVLO -SENSE, GND VOADJ) — R955 DNI 0603 — R958 8.2K 0603 — C1091 0402 — C1092 1210 — C1093 SMC_EL_FP_G — 1.4v–PreFilter — L158 — PM3700-10-RC — L156 10uH mss1210 — L157 DNI SML-DM3312 — L159 10uH mss1210 — L160 100 ohms 100 MHz SML-DM3312 — C1096 0.1uF 0402 — C1097 22uF 1210 — C1098 560uF SMC_EL_FP_G — 1.4v–PostFilter — C2365 10uF — C2366 10uF — C2367 470uF — U274 VIN1 VIN2 VOUT1 VOUT2 EN ADJ GND TABGND — MIC69502WR — Set for 0.4V drop — 1.0V — R1222 1.00K — R1223 1.00K — C2368 470uF — C2369 10uF — C2370 100uF 1210

5V–PreFilter — C1094 22uF 1210 — C1095 0.1uF 0402 — SYNC2 — U104 PTH04T260WAD — R956 DNI 0603 — R759 4.53K 0603 — C973 0.1uF 0402 — C606 22uF 1210 — C611 560uF smc_el_fp_g — 1.8v–PreFilter — L103 — PM3700-10-RC — L95 10uH mss1210 — L83 DNI SML-DM3312 — L94 10uH mss1210 — L82 100 ohms 100 MHz SML-DM3312 — C590 0.1uF 0402 — C596 22uF 1210 — C584 560uF smc_el_fp_g — L75 100 ohms 100 MHz SML-DM3312 — L74 100 ohms 100 MHz SML-DM3312 — C576 0.1uF 0402 — C579 22uF 1210 — C573 560uF smc_el_fp_g — 1.8V_A — 1.8V — VTP22 TP_WHT — AGND

5V–PreFilter — C1066 0.1uF 0402 — PWRGND — 5V–PreFilter — U150 DIV PH MOD SET V+ GND OUT1 OUT2 OUT3 OUT4 — LTC6902CMS#PBF — R866 0 SYNC1 — R867 0 SYNC2 — R868 0 SYNC3 — R869 0 SYNC4 — R863 0 0603 — R864 DNI 0603 — R865 165K 0603 — R870 0 0603 — R871 DNI 0603 — R872 0 0603 — PWRGND

5V–PreFilter — C620 22uF 1210 — C975 0.1uF 0402 — SYNC3 — U105 PTH04T260WAD — R755 DNI 0603 — R758 2.21K 0603 — C972 0.1uF 0402 — C607 22uF 1210 — C612 560uF SMC_EL_FP_G — 2.5v–PreFilter — L104 — PM3700-10-RC — L97 10uH mss1210 — L85 DNI SML-DM3312 — L96 10uH mss1210 — L84 100 ohms 100 MHz SML-DM3312 — C591 0.1uF 0402 — C597 22uF 1210 — C585 560uF SMC_EL_FP_G — 2.5V — AGND

Bill of Materials Item
100 ohms 100 MHz
External to PC Board
X L85

Bill of Materials Item
100 ohms 100 MHz
External to PC Board
X L81

5V–PreFilter — C618 22uF 1210 — C977 0.1uF 0402 — SYNC4 — U103 PTH04T260WAD — R757 DNI 0603 — R760 1.15K 0603 — C974 0.1uF 0402 — C605 22uF 1210 — C610 560uF smc_el_fp_g — 3.3v–PreFilter — L102 — PM3700-10-RC — L93 10uH mss1210 — L81 DNI SML-DM3312 — L92 10uH mss1210 — L80 100 ohms 100 MHz SML-DM3312 — C589 0.1uF 0402 — C595 22uF 1210 — C583 560uF SMC_EL_FP_G — L73 100 ohms 100 MHz SML-DM3312 — L72 100 ohms 100 MHz SML-DM3312 — C575 0.1uF 0402 — C578 22uF 1210 — C572 560uF smc_el_fp_g — 3.3V_A — 3.3V — VTP23 TP_WHT — AGND

5V–PreFilter — C617 22uF 1210 — C621 0.1uF 0402 — U106 CC3-0503SF-E (+Vin, SHDN-Bar, -Vin, +Vout, NC6, -Vout, NC4) — R962 DNI — C971 0.1uF 0402 — C604 22uF 1210 — C609 560uF SMC_EL_FP_G — -3.3v–PreFilter — L101 — PM3700-10-RC — L91 10uH mss1210 — L79 100 ohms 100 MHz SML-DM3312 — L90 10uH mss1210 — L78 DNI SML-DM3312 — C2466 0.1uF 0402 — C2467 22uF 1210 — C588 0.1uF 0402 — C594 22uF 1210 — C582 560uF smc_el_fp_g — AGND

could U106 be driven from 5.0V_A so that if the +5 dies so too will the -5?

negative rail for input op-amps

-V_A — VTP1 TP_BRN

Bill of Materials Item
DDPAK HEAT SINK
External to PC Board
X-U158

Bill of Materials Item
100 ohms 100 MHz
External to PC Board
X L78

U158 OUT SENSE/ADJ IN-1 IN-2 GND NSHDN — LT3015EQ#PBF — R975 4.02K 1206 — R976 10.0K 0603 — AGND

tie pin 6 to copper fill for heat-sink

3.3V — Temperature monitor for U158 — U296 SCL SDA V+ ADD0 ADD1 GND — TMP100NA/3K — C2472 0.1uF 0402 — TEMPMON_SCL TEMPMON_SDA — ADD1 | ADD0 | SLAVE ADDRESS 1 | FLT | 1001101

SSP TEST POINT COLOR CODING

SIGNAL	COLOR
Power GND	GREEN
Digital GND	BLACK
Analog GND	GRAY
+3.3V	RED
+2.5V	ORANGE
+1.8V	BLUE
+1.35V	YELLOW
+1.0V	WHITE
Clocks	PURPLE
Misc.	BROWN

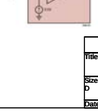
3.3V VTP2 TP_RED — 2.5V VTP3 TP_ORG — 1.8V VTP4 TP_BLU — 1.0V VTP6 TP_WHT — 5.0V VTP12 TP_BRN — 5.0V_A VTP13 TP_BRN — 5V–PreFilter Vbias VTP14 TP_BRN — Vbias_EXT VTP15 TP_BRN — VTP16

1.0V — R315 86.6K 0603 — R316 100K 0603 — 1.4v–PostFilter — 2.5V — 1.8V — R324 162K 0603 — R325 100K 0603 — 5.0V — 3.3V — U98 V1 6.0V (4.675V) V2 3.3V (3.166V) V3 2.5V (2.338V) V4 1.8V (1.683V) VADJ1 VADJ2 GND RST — LTC2908ITS8-A1#TRMPBF — R326 200 0603 — POWER_GOOD

POWER_GOOD is low until all inputs are within tolerance and have stayed so for 200ms.

Table 1. Suggested 1% Resistor Values for the V_{OUT} Inputs

$V_{OUT(nom)}$ (V)	V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
12	11.25	2150	180
10	9.4	1780	180
8	7.5	1400	180
7.5	7	1300	180
6	5.6	1020	180
5	4.725	845	180
3.3	3.055	511	180
3	2.82	464	180
2.5	2.329	365	180
1.8	1.685	237	180
1.5	1.410	182	180
1.2	1.120	124	180
1.0	0.933	86.6	180
0.9	0.840	68.1	180
0.8	0.750	49.9	180
0.7	0.650	30.9	180
0.6	0.561	12.1	180



SSP_BOT_SHIELD — S1 MuMetal Bottom Shield ProtoDUNE SSP — PWRGND

SSP_TOP_SHIELD — S2 MuMetal Top Shield ProtoDUNE SSP — PWRGND

Sync chip settings

Rset = 20k * (10M / (N * M * fout))
fMASTER = 10M * (20k / Rset)

Rset Range = 10k to 2M
fMASTER Range = 100kHz to 20 MHz

N = 100 if DIV pin = V+
N = 10 if DIV pin = Open
N = 1 if DIV pin = GND

M = 4 if PH Pin = V+ (4 Phase Output)
M = 3 if PH Pin = Open (3 Phase Output)
M = 1 if PH Pin = GND (2 Phase Output)

2 Phase Mode:
OUT 1 & 3 = 0 deg.
OUT 2 & 4 = 180 deg.

3 Phase Mode:
OUT 1 = 0 deg
OUT 2 = 120 deg.
OUT 3 = 240 deg.
OUT 4 = Disabled.

4 Phase Mode:
OUT 1 = 0 deg
OUT 2 = 90 deg.
OUT 3 = 180 deg.
OUT 4 = 270 deg.

Modulation is disabled by connecting MOD to GND.

0.5 AMP/5 VOLT DC — 5V–PreFilterF4 — SF-1206S050-2 — J38 — 22-29-2021
0.5 AMP/5 VOLT DC — F6 — SF-1206S050-2 — J58 — 22-29-2021
0.5 AMP/5 VOLT DC — F7 — SF-1206S050-2 — J61 — 22-29-2021
0.5 AMP/5 VOLT DC — F8 — SF-1206S050-2 — J62 — 22-29-2021
PWRGND

R231 R720 R721 R722 R723 R724 R725 R726 R727 R728 R729 R730 DNI — AGND

AG13 AG14 AG15 AG16 TP_GRY — PG1 PG2 TP_GRN — DG1 DG2 DG3 DG4 DG5 DG6 DG7 TP_BLK

XC7A200T XADC — U92-25 — U18 — TP5 — TP4 — V17 — xc7a200t_ffg1156 — U17

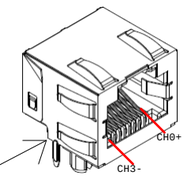
Title	PowerSupply		
Size D	Document Number PC17001A		Rev A
Date: Monday, June 05, 2017	Sheet 29 of 35		

OUTSIDE THE SSP

INSIDE THE SSP

Cable enters this way in PCB layout view

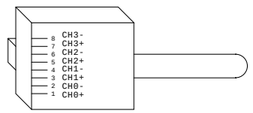
Since cable end is shown with locking tab AWAY, when rotated to match RJ45 socket pin 8 (CH3+) is the pin at left, pin 1 (CH0-) is the pin at right.



PCB layout pattern of connector to right

Anderson understanding of cable pinout from RearCon page of schematic

Pin numbers appear to match but polarity and channel number uncertain.



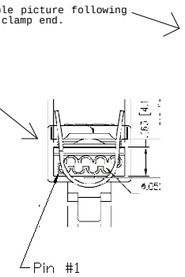
Connector at right must rotate to align latch with socket.

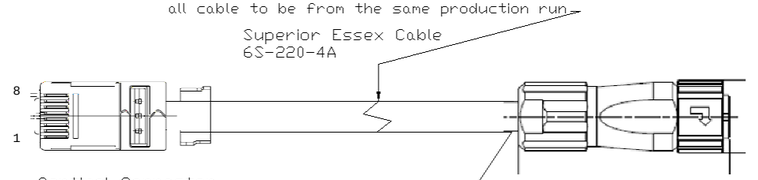
Tim Cundiff cable drawing

all cable to be from the same production run

Superior Essex Cable
6S-220-4A

Numbering transferred to cable picture following pin 1 ID in view from cable clamp end.



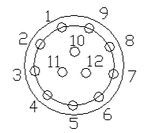


Sentinel Connector
111S08080091H34

1	Blue	1
2	Blue/Wht	2
3	Brown	3
4	Brown/Wht	4
5	Green	6
6	Green/Wht	7
7	Orange	8
8	Orangw/Wht	9

5,10,11,12 not used

Hirose Electric connector
LF10WBP-12S



Looking at solder side

SSP Channel 3

SSP Channel 2

SSP Channel 1

SSP Channel 0

Due to the way the connector is numbered relative to the way the channel stripes in the SSP are laid out - caused by the connector being in the rear of the box - SSP channel 0 is actually connected to cable channel 3.

Care is thus required to ensure that SSP channel number and cable channel number are not confused.

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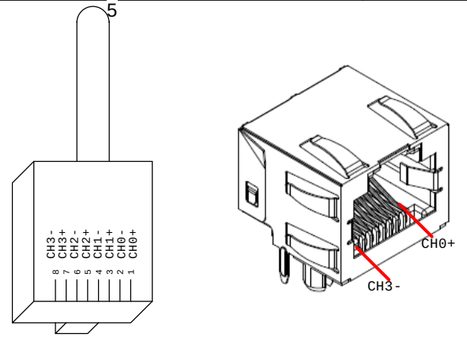
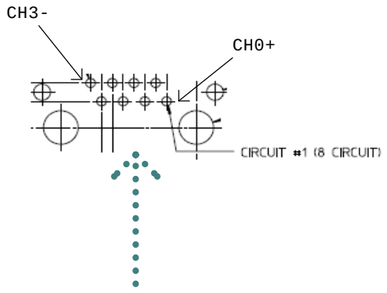
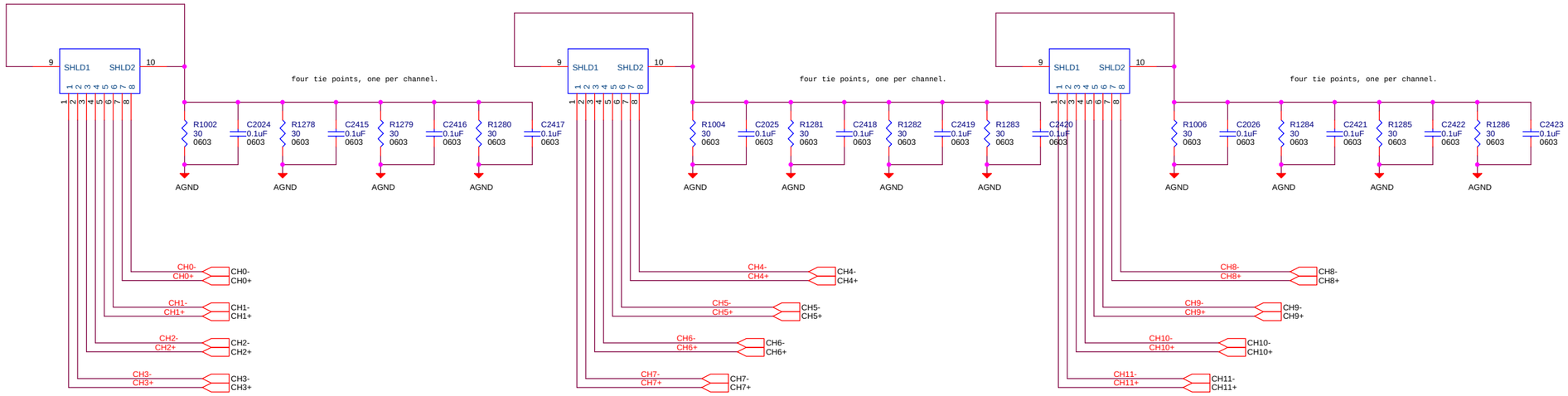
Rear Panel RJ45 Connectors to Channels 0 to 11





Cable enters this way in PCB layout view



Layout issue not addressed in prototype ECOs

Polarity of RJ45 pairs swapped relative to expectations. + and - of each channel swapped here by flipping the ports in pairs relative to the prototype and as-built.

SFP interface to timing system

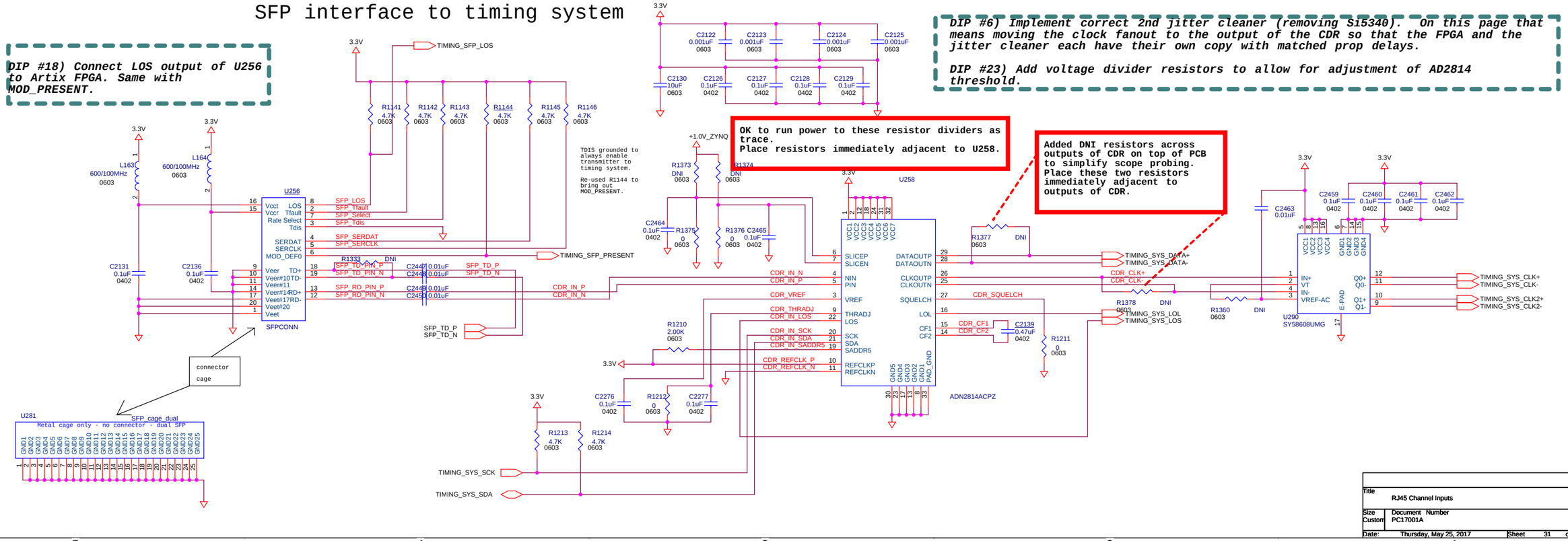
DIP #18) Connect LOS output of U256 to Artix FPGA. Same with MOD_PRESENT.

DIP #6) Implement correct 2nd jitter cleaner (removing Si5340). On this page that means moving the clock fanout to the output of the CDR so that the FPGA and the jitter cleaner each have their own copy with matched prop delays.

DIP #23) Add voltage divider resistors to allow for adjustment of AD2814 threshold.

OK to run power to these resistor dividers as trace.
Place resistors immediately adjacent to U258.

Added DNI resistors across outputs of CDR on top of PCB to simplify scope probing. Place these two resistors immediately adjacent to outputs of CDR.



Title	RJ45 Channel Inputs		
Size Custom	Document Number PC17001A		Rev A
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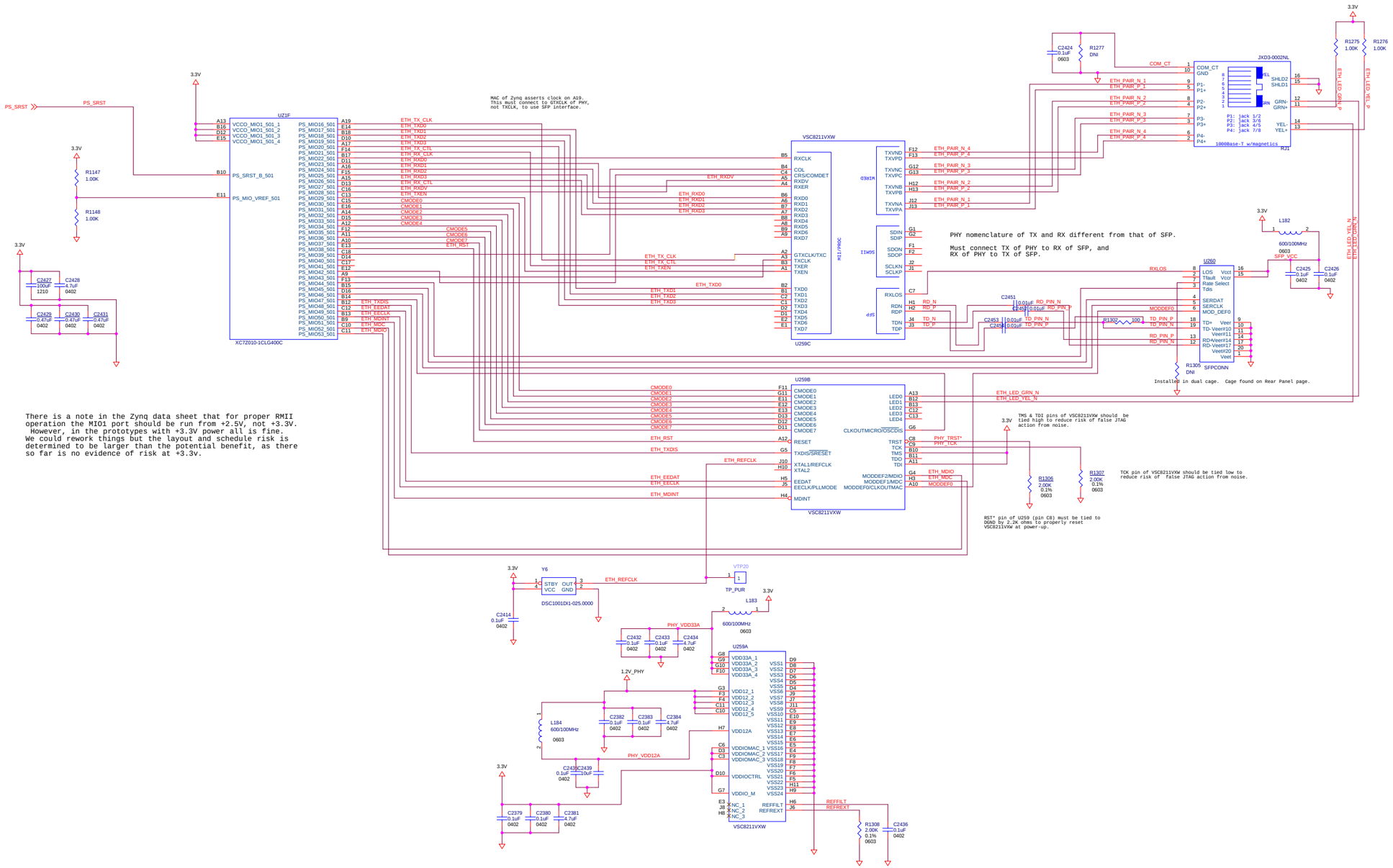

Title	<Title>
Size: D	Document Number: PC17001A
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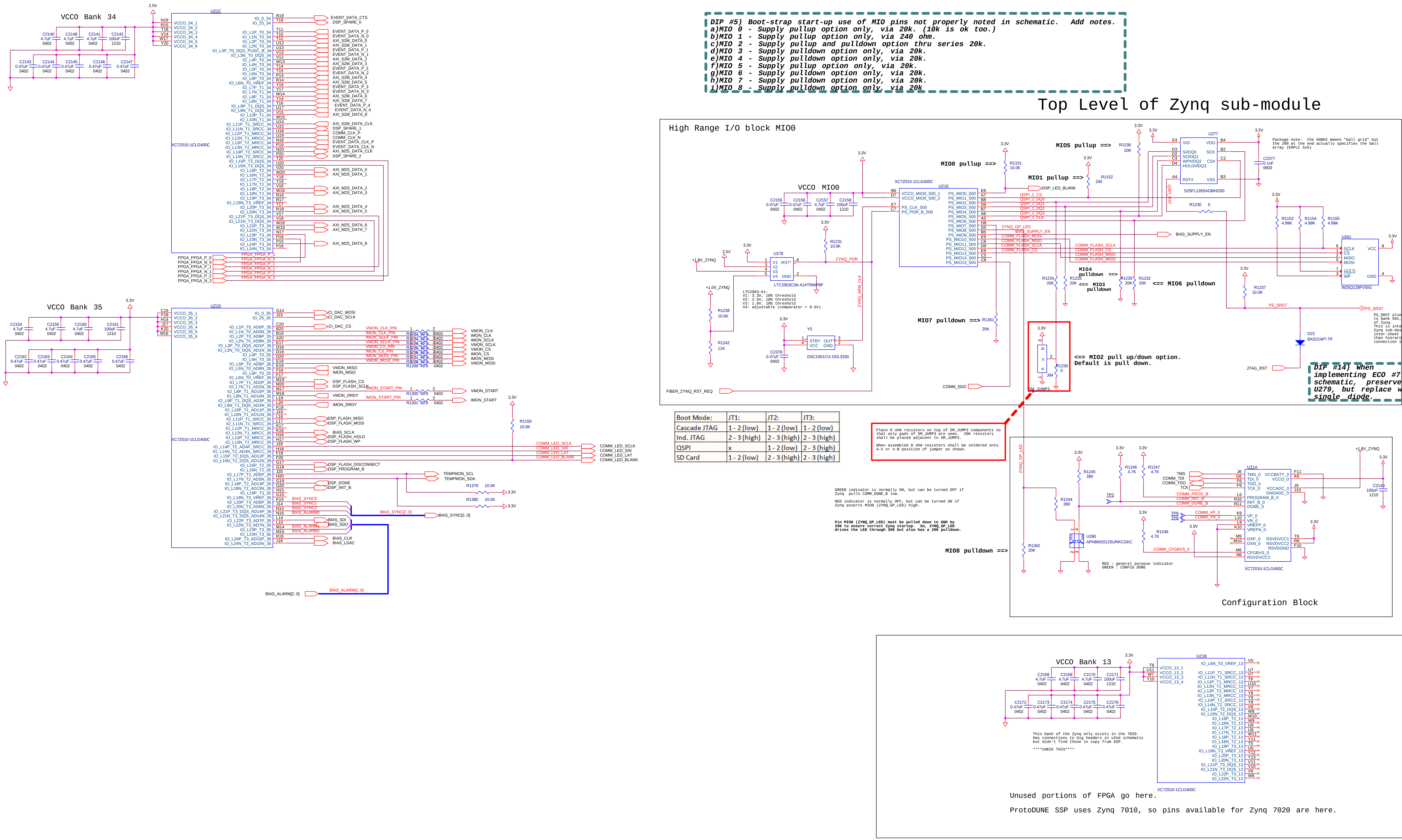
Top Level of Zynq sub-module



DIP #5) Boot-strap start-up use of MIO pins not properly noted in schematic. Add notes.
a)MIO 0 - Supply pullup option only, via 20k. (10k is ok too.)
b)MIO 1 - Supply pullup option only, via 240 ohm.
c)MIO 2 - Supply pullup and pulldown option thru series 20k.
d)MIO 3 - Supply pulldown option only, via 20k.
e)MIO 4 - Supply pulldown option only, via 20k.
f)MIO 5 - Supply pullup option only, via 20k.
g)MIO 6 - Supply pulldown option only, via 20k.
h)MIO 7 - Supply pulldown option only, via 20k.
i)MIO 8 - Supply pulldown option only, via 20k

Package note: the AGBHI means "ball grid" but the 200 at the end actually specifies the ball array (EHPLC 5x5)

PS_SRST also connects to bank 501, PS_SRST of Zynq. This is internal to Zynq sub-design so inter-sheet rather than hierarchical connection is used.

DIP #14) When implementing ECO #7 in schematic, preserve U279, but replace with single diode.

Boot Mode:	JT1:	JT2:	JT3:
Cascade JTAG	1 - 2 (low)	1 - 2 (low)	1 - 2 (low)
Ind. JTAG	2 - 3 (high)	2 - 3 (high)	2 - 3 (high)
QSPI	x	1 - 2 (low)	2 - 3 (high)
SD Card	1 - 2 (low)	2 - 3 (high)	2 - 3 (high)

Place 0 ohm resistors on top of SM_JUMP3 components so that only pads of SM_JUMP3 are seen. 20K resistors shall be placed adjacent to SM_JUMP3.

When assembled 0 ohm resistors shall be soldered onto A-X or X-B position of jumper as shown.

GREEN indicator is normally ON, but can be turned OFF if Zynq pulls COMM_DONE_B low.

RED indicator is normally OFF, but can be turned ON if Zynq asserts MIO8 (ZYNQ_GP_LED) high.

Pin MIO8 (ZYNQ_GP_LED) must be pulled down to GND by 20K to ensure correct Zynq startup. So, ZYNQ_GP_LED drives the LED through 390 but also has a 20K pulldown.

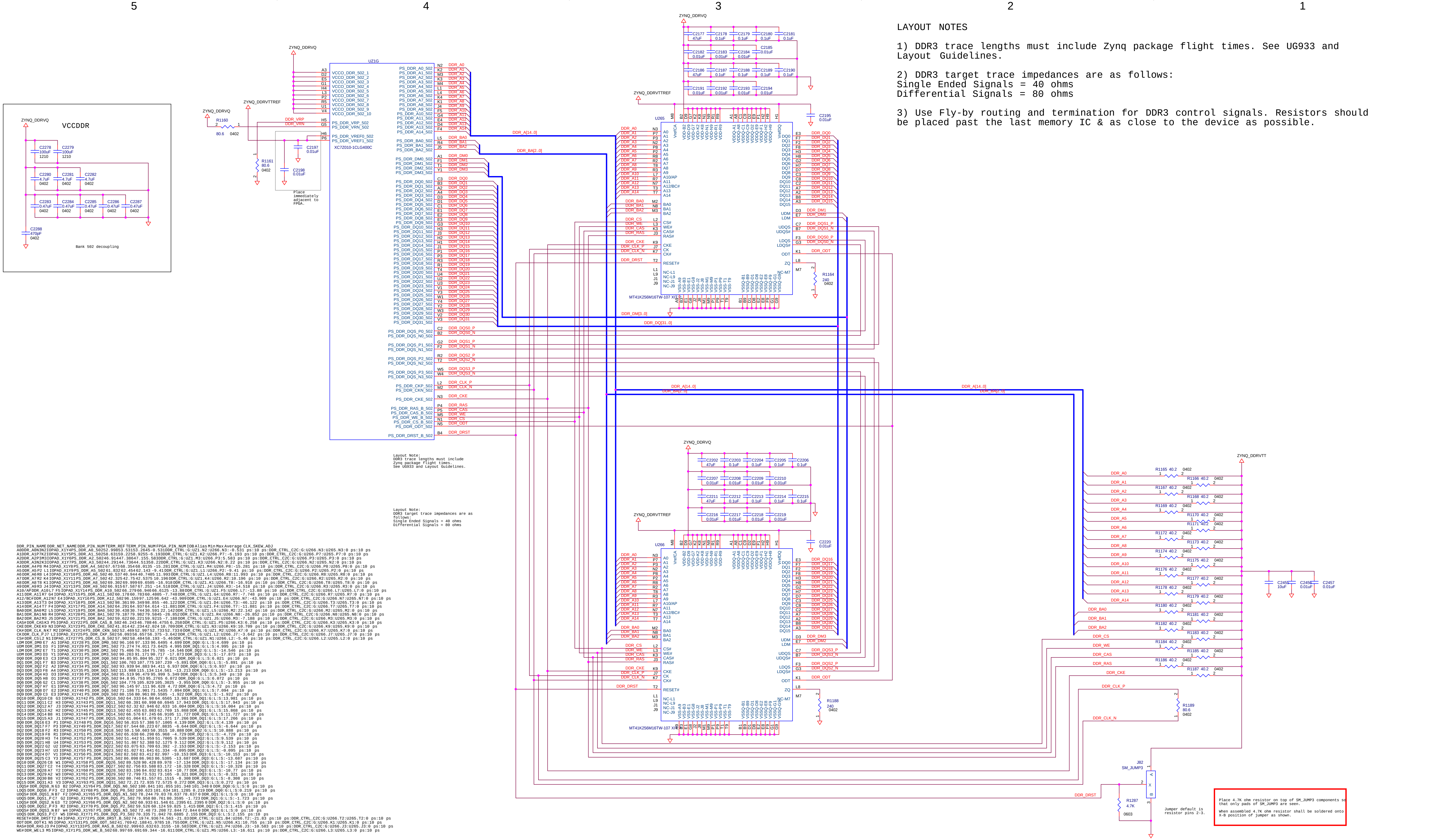
RED : general purpose indicator
GREEN : CONFIG DONE

This bank of the Zynq only exists in the 7020. Has connections to big headers in uZed schematic but didn't find those in copy from SSP.

****CHECK THIS****

Unused portions of FPGA go here.

ProtoDUNE SSP uses Zynq 7010, so pins available for Zynq 7020 are here.



LAYOUT NOTES

1) DDR3 trace lengths must include Zynq package flight times. See UG933 and Layout Guidelines.

2) DDR3 target trace impedances are as follows:
Single Ended Signals = 40 ohms
Differential Signals = 80 ohms

3) Use Fly-by routing and termination for DDR3 control signals. Resistors should be placed past the last memory IC & as close to the device as possible.

Layout Note:
DDR3 trace lengths must include Zynq package flight times.
See UG933 and Layout Guidelines.

Layout Note:
DDR3 target trace impedances are as follows:
Single Ended Signals = 40 ohms
Differential Signals = 80 ohms

```
DDR_PIN_NAME DDR_NET_NAME DDR_PIN_NUM TERM_REF TERM_PIN_NUM FPGA_PIN_NUM IOB Alias Min Max Average CLK_SKEW_ADJ
A0DDR_A0N3N2IOPAD_X1Y4PS_DDR_A0_50252.99853.53153.2645-0.531DDR_CTRL:G:UZ1.N2:U266.N3:-0.531 ps:10 ps:DDR_CTRL_C2C:G:U266.N3:U265.N3:0 ps:10 ps
A1DDR_A1P7K2IOPAD_X1Y5PS_DDR_A1_50258.63159.2258.9255-6.193DDR_CTRL:G:UZ1.K2:U266.P7:-6.193 ps:10 ps:DDR_CTRL_C2C:G:U266.P7:U265.P7:0 ps:10 ps
A2DDR_A2P3M3IOPAD_X1Y6PS_DDR_A2_50246.91447.38647.155.583DDR_CTRL:G:UZ1.M3:U266.P3:5.583 ps:10 ps:DDR_CTRL_C2C:G:U266.P3:U265.P3:0 ps:10 ps
A3DDR_A3N2K3IOPAD_X1Y7PS_DDR_A3_50244.29144.73644.51358.22DDR_CTRL:G:UZ1.K3:U266.N2:8.22 ps:10 ps:DDR_CTRL_C2C:G:U266.N2:U265.N2:0 ps:10 ps
A4 DDR_A4 P8 M4 IOPAD_X1Y8 PS_DDR_A4_502 67.673 68.354 68.0135 -15.281 DDR_CTRL:G:UZ1.M4:U266.P8:-15.281 ps:10 ps:DDR_CTRL_C2C:G:U266.P8:U265.P8:0 ps:10 ps
A5 DDR_A5 P2 L1 IOPAD_X1Y9 PS_DDR_A5_502 61.832 62.454 62.143 -9.41 DDR_CTRL:G:UZ1.L1:U266.P2:-9.41 ps:10 ps:DDR_CTRL_C2C:G:U266.P2:U265.P2:0 ps:10 ps
A6 DDR_A6 R8 L4 IOPAD_X1Y10 PS_DDR_A6_502 40.537 40.944 40.7405 11.993 DDR_CTRL:G:UZ1.L4:U266.R8:11.993 ps:10 ps:DDR_CTRL_C2C:G:U266.R8:U265.R8:0 ps:10 ps
A7 DDR_A7 R2 K4 IOPAD_X1Y11 PS_DDR_A7_502 42.325 42.75 42.5375 10.196 DDR_CTRL:G:UZ1.K4:U266.R2:10.196 ps:10 ps:DDR_CTRL_C2C:G:U266.R2:U265.R2:0 ps:10 ps
A8 DDR_A8 T8 K1 IOPAD_X1Y12 PS_DDR_A8_502 69.302 69.999 69.6505 -16.918 DDR_CTRL:G:UZ1.K1:U266.T8:-16.918 ps:10 ps:DDR_CTRL_C2C:G:U266.T8:U265.T8:0 ps:10 ps
A9 DDR_A9 R3 J4 IOPAD_X1Y13 PS_DDR_A9_502 66.915 67.587 67.251 -14.518 DDR_CTRL:G:UZ1.J4:U266.R3:-14.518 ps:10 ps:DDR_CTRL_C2C:G:U266.R3:U265.R3:0 ps:10 ps
A10/AP DDR_A10 L7 F5 IOPAD_X1Y14 PS_DDR_A10_502 66.279 66.946 66.6125 -13.88 DDR_CTRL:G:UZ1.F5:U266.L7:-13.88 ps:10 ps:DDR_CTRL_C2C:G:U266.L7:U265.L7:0 ps:10 ps
A11 DDR_A11 R7 G4 IOPAD_X1Y15 PS_DDR_A11_502 60.178 60.783 60.4805 -7.748 DDR_CTRL:G:UZ1.G4:U266.R7:-7.748 ps:10 ps:DDR_CTRL_C2C:G:U266.R7:U265.R7:0 ps:10 ps
A12/BC# DDR_A12 N7 E4 IOPAD_X1Y16 PS_DDR_A12_502 96.159 97.125 96.642 -43.909 DDR_CTRL:G:UZ1.E4:U266.N7:-43.909 ps:10 ps:DDR_CTRL_C2C:G:U266.N7:U265.N7:0 ps:10 ps
A13 DDR_A13 T3 D4 IOPAD_X1Y18 PS_DDR_A13_502 98.361 99.349 98.855 -46.122 DDR_CTRL:G:UZ1.D4:U266.T3:-46.122 ps:10 ps:DDR_CTRL_C2C:G:U266.T3:U265.T3:0 ps:10 ps
A14 DDR_A14 T7 F4 IOPAD_X1Y17 PS_DDR_A14_502 64.291 64.937 64.614 -11.881 DDR_CTRL:G:UZ1.F4:U266.T7:-11.881 ps:10 ps:DDR_CTRL_C2C:G:U266.T7:U265.T7:0 ps:10 ps
BA0 DDR_BA0 M2 L5 IOPAD_X1Y19 PS_DDR_BA0_502 30.438 30.744 30.591 22.142 DDR_CTRL:G:UZ1.L5:U266.M2:22.142 ps:10 ps:DDR_CTRL_C2C:G:U266.M2:U265.M2:0 ps:10 ps
BA1 DDR_BA1 N8 R4 IOPAD_X1Y20 PS_DDR_BA1_502 79.187 79.982 79.5845 -26.852 DDR_CTRL:G:UZ1.R4:U266.N8:-26.852 ps:10 ps:DDR_CTRL_C2C:G:U266.N8:U265.N8:0 ps:10 ps
BA2 DDR_BA2 M3 J5 IOPAD_X1Y21 PS_DDR_BA2_502 59.622 60.221 59.9215 -7.188 DDR_CTRL:G:UZ1.J5:U266.M3:-7.188 ps:10 ps:DDR_CTRL_C2C:G:U266.M3:U265.M3:0 ps:10 ps
CAS# DDR_CAS K3 P5 IOPAD_X1Y22 PS_DDR_CAS_B_502 46.243 46.708 46.4755 6.258 DDR_CTRL:G:UZ1.P5:U266.K3:6.258 ps:10 ps:DDR_CTRL_C2C:G:U266.K3:U265.K3:0 ps:10 ps
CKE DDR_CKE K9 N3 IOPAD_X1Y23 PS_DDR_CKE_502 41.814 42.234 42.024 10.709 DDR_CTRL:G:UZ1.N3:U266.K9:10.709 ps:10 ps:DDR_CTRL_C2C:G:U266.K9:U265.K9:0 ps:10 ps
CK# DDR_CLK_N K7 M2 IOPAD_X1Y24 PS_DDR_CKN_502 52.469 52.997 52.733 52.733 0 DDR_CTRL:G:UZ1.M2:U266.K7:0 ps:10 ps:DDR_CTRL_C2C:G:U266.K7:U265.K7:0 ps:10 ps
CK DDR_CLK_P J7 L2 IOPAD_X1Y25 PS_DDR_CKP_502 56.093 56.657 56.375 -3.642 DDR_CTRL:G:UZ1.L2:U266.J7:-3.642 ps:10 ps:DDR_CTRL_C2C:G:U266.J7:U265.J7:0 ps:10 ps
CS# DDR_CS L2 N1 IOPAD_X1Y27 PS_DDR_CS_B_502 57.902 58.484 58.193 -5.46 DDR_CTRL:G:UZ1.N1:U266.L2:-5.46 ps:10 ps:DDR_CTRL_C2C:G:U266.L2:U265.L2:0 ps:10 ps
LDM DDR_DM0 E7 A1 IOPAD_X1Y28 PS_DDR_DM0_502 96.166 97.133 96.6495 4.699 DDR_DQ0:G:L:S:4.699 ps:10 ps
UDM DDR_DM1 D3 F1 IOPAD_X1Y29 PS_DDR_DM1_502 73.274 74.011 73.6425 4.995 DDR_DQ1:G:L:S:4.995 ps:10 ps
LDM DDR_DM2 E7 T1 IOPAD_X1Y30 PS_DDR_DM2_502 75.406 76.164 75.785 -14.546 DDR_DQ2:G:L:S:-14.546 ps:10 ps
UDM DDR_DM3 D3 Y1 IOPAD_X1Y31 PS_DDR_DM3_502 90.263 91.171 90.717 -17.873 DDR_DQ3:G:L:S:-17.873 ps:10 ps
DQ0 DDR_DQ0 E3 C3 IOPAD_X1Y32 PS_DDR_DQ0_502 94.85 95.804 95.327 6.021 DDR_DQ0:G:L:S:6.021 ps:10 ps
DQ1 DDR_DQ1 F7 B3 IOPAD_X1Y33 PS_DDR_DQ1_502 106.703 107.775 107.239 -5.891 DDR_DQ0:G:L:S:-5.891 ps:10 ps
DQ2 DDR_DQ2 F2 A2 IOPAD_X1Y34 PS_DDR_DQ2_502 93.939 94.883 94.411 6.937 DDR_DQ0:G:L:S:6.937 ps:10 ps
DQ3 DDR_DQ3 F8 A4 IOPAD_X1Y35 PS_DDR_DQ3_502 113.988 115.134 114.561 -13.213 DDR_DQ0:G:L:S:-13.213 ps:10 ps
DQ4 DDR_DQ4 H3 D3 IOPAD_X1Y36 PS_DDR_DQ4_502 95.519 96.479 95.999 5.349 DDR_DQ0:G:L:S:5.349 ps:10 ps
DQ5 DDR_DQ5 H8 D1 IOPAD_X1Y37 PS_DDR_DQ5_502 94.8 95.753 95.2765 6.072 DDR_DQ0:G:L:S:6.072 ps:10 ps
DQ6 DDR_DQ6 G2 C1 IOPAD_X1Y38 PS_DDR_DQ6_502 104.776 105.829 105.3025 -3.955 DDR_DQ0:G:L:S:-3.955 ps:10 ps
DQ7 DDR_DQ7 H7 E1 IOPAD_X1Y39 PS_DDR_DQ7_502 96.145 97.111 96.628 4.72 DDR_DQ0:G:L:S:4.72 ps:10 ps
DQ8 DDR_DQ8 D7 E2 IOPAD_X1Y40 PS_DDR_DQ8_502 71.186 71.901 71.5435 7.094 DDR_DQ1:G:L:S:7.094 ps:10 ps
DQ9 DDR_DQ9 C3 E3 IOPAD_X1Y41 PS_DDR_DQ9_502 80.156 80.961 80.5585 -1.922 DDR_DQ1:G:L:S:-1.922 ps:10 ps
DQ10 DDR_DQ10 C8 G3 IOPAD_X1Y42 PS_DDR_DQ10_502 64.333 64.98 64.6565 13.981 DDR_DQ1:G:L:S:13.981 ps:10 ps
DQ11 DDR_DQ11 C2 H3 IOPAD_X1Y43 PS_DDR_DQ11_502 60.391 60.998 60.6945 17.943 DDR_DQ1:G:L:S:17.943 ps:10 ps
DQ12 DDR_DQ12 A7 J3 IOPAD_X1Y44 PS_DDR_DQ12_502 62.32 62.946 62.633 16.004 DDR_DQ1:G:L:S:16.004 ps:10 ps
DQ13 DDR_DQ13 A2 H2 IOPAD_X1Y45 PS_DDR_DQ13_502 62.455 63.083 62.769 15.868 DDR_DQ1:G:L:S:15.868 ps:10 ps
DQ14 DDR_DQ14 B8 H1 IOPAD_X1Y46 PS_DDR_DQ14_502 66.576 67.245 66.9105 11.727 DDR_DQ1:G:L:S:11.727 ps:10 ps
DQ15 DDR_DQ15 A3 J1 IOPAD_X1Y47 PS_DDR_DQ15_502 61.064 61.678 61.371 17.266 DDR_DQ1:G:L:S:17.266 ps:10 ps
DQ0 DDR_DQ16 E3 P1 IOPAD_X1Y48 PS_DDR_DQ16_502 56.815 57.386 57.1005 4.139 DDR_DQ2:G:L:S:4.139 ps:10 ps
DQ1 DDR_DQ17 F7 P3 IOPAD_X1Y49 PS_DDR_DQ17_502 67.544 68.223 67.8835 -6.644 DDR_DQ2:G:L:S:-6.644 ps:10 ps
DQ2 DDR_DQ18 F2 R3 IOPAD_X1Y50 PS_DDR_DQ18_502 50.1 50.603 50.3515 10.888 DDR_DQ2:G:L:S:10.888 ps:10 ps
DQ3 DDR_DQ19 F8 R1 IOPAD_X1Y51 PS_DDR_DQ19_502 65.638 66.298 65.968 -4.729 DDR_DQ2:G:L:S:-4.729 ps:10 ps
DQ4 DDR_DQ20 H3 T4 IOPAD_X1Y52 PS_DDR_DQ20_502 51.442 51.959 51.7005 9.539 DDR_DQ2:G:L:S:9.539 ps:10 ps
DQ5 DDR_DQ21 H8 U4 IOPAD_X1Y53 PS_DDR_DQ21_502 51.867 52.388 52.1275 9.112 DDR_DQ2:G:L:S:9.112 ps:10 ps
DQ6 DDR_DQ22 G2 U2 IOPAD_X1Y54 PS_DDR_DQ22_502 63.075 63.709 63.392 -2.153 DDR_DQ2:G:L:S:-2.153 ps:10 ps
DQ7 DDR_DQ23 H7 U3 IOPAD_X1Y55 PS_DDR_DQ23_502 61.027 61.641 61.334 -0.095 DDR_DQ2:G:L:S:-0.095 ps:10 ps
DQ8 DDR_DQ24 D7 V1 IOPAD_X1Y56 PS_DDR_DQ24_502 82.582 83.412 82.997 -10.153 DDR_DQ3:G:L:S:-10.153 ps:10 ps
DQ9 DDR_DQ25 C3 Y3 IOPAD_X1Y57 PS_DDR_DQ25_502 86.098 86.963 86.5305 -13.687 DDR_DQ3:G:L:S:-13.687 ps:10 ps
DQ10 DDR_DQ26 C8 W1 IOPAD_X1Y58 PS_DDR_DQ26_502 89.528 90.428 89.978 -17.134 DDR_DQ3:G:L:S:-17.134 ps:10 ps
DQ11 DDR_DQ27 C2 Y4 IOPAD_X1Y59 PS_DDR_DQ27_502 82.756 83.588 83.172 -10.328 DDR_DQ3:G:L:S:-10.328 ps:10 ps
DQ12 DDR_DQ28 A7 Y2 IOPAD_X1Y60 PS_DDR_DQ28_502 83.196 84.032 83.614 -10.77 DDR_DQ3:G:L:S:-10.77 ps:10 ps
DQ13 DDR_DQ29 A2 W3 IOPAD_X1Y61 PS_DDR_DQ29_502 72.799 73.531 73.165 -0.321 DDR_DQ3:G:L:S:-0.321 ps:10 ps
DQ14 DDR_DQ30 B8 V2 IOPAD_X1Y62 PS_DDR_DQ30_502 80.746 81.557 81.1515 -8.308 DDR_DQ3:G:L:S:-8.308 ps:10 ps
DQ15 DDR_DQ31 A3 V3 IOPAD_X1Y63 PS_DDR_DQ31_502 72.21 72.935 72.5725 0.272 DDR_DQ3:G:L:S:0.272 ps:10 ps
LDQS# DDR_DQS0_N G3 B2 IOPAD_X1Y64 PS_DDR_DQS_N0_502 100.841 101.855 101.348 101.348 0 DDR_DQ0:G:L:S:0 ps:10 ps
LDQS DDR_DQS0_P F3 C2 IOPAD_X1Y68 PS_DDR_DQS_P0_502 100.623 101.634 101.1285 0.219 DDR_DQ0:G:L:S:0.219 ps:10 ps
UDQS# DDR_DQS1_N B7 F2 IOPAD_X1Y65 PS_DDR_DQS_N1_502 78.244 79.03 78.637 78.637 0 DDR_DQ1:G:L:S:0 ps:10 ps
UDQS DDR_DQS1_P C7 G2 IOPAD_X1Y69 PS_DDR_DQS_P1_502 79.958 80.761 80.3595 -1.723 DDR_DQ1:G:L:S:-1.723 ps:10 ps
LDQS# DDR_DQS2_N G3 T2 IOPAD_X1Y66 PS_DDR_DQS_N2_502 60.933 61.546 61.2395 61.2395 0 DDR_DQ2:G:L:S:0 ps:10 ps
LDQS DDR_DQS2_P F3 R2 IOPAD_X1Y70 PS_DDR_DQS_P2_502 59.526 60.124 59.825 1.415 DDR_DQ2:G:L:S:1.415 ps:10 ps
UDQS# DDR_DQS3_N B7 W4 IOPAD_X1Y67 PS_DDR_DQS_N3_502 72.48 73.208 72.844 72.844 0 DDR_DQ3:G:L:S:0 ps:10 ps
UDQS DDR_DQS3_P C7 W5 IOPAD_X1Y71 PS_DDR_DQS_P3_502 70.335 71.042 70.6885 2.155 DDR_DQ3:G:L:S:2.155 ps:10 ps
RESET# DDR_DRST T2 B4 IOPAD_X1Y72 PS_DDR_DRST_B_502 74.19 74.936 74.563 -21.83 DDR_CTRL:G:UZ1.B4:U266.T2:-21.83 ps:10 ps:DDR_CTRL_C2C:G:U266.T2:U265.T2:0 ps:10 ps
ODT DDR_ODT K1 N5 IOPAD_X1Y131 PS_DDR_ODT_502 41.769 42.188 41.9785 10.755 DDR_CTRL:G:UZ1.N5:U266.K1:10.755 ps:10 ps:DDR_CTRL_C2C:G:U266.K1:U265.K1:0 ps:10 ps
RAS# DDR_RAS J3 P4 IOPAD_X1Y133 PS_DDR_RAS_B_502 62.999 63.632 63.3155 -10.583 DDR_CTRL:G:UZ1.P4:U266.J3:-10.583 ps:10 ps:DDR_CTRL_C2C:G:U266.J3:U265.J3:0 ps:10 ps
WE# DDR_WE L3 M5 IOPAD_X1Y1 PS_DDR_WE_B_502 68.997 69.691 69.344 -16.611 DDR_CTRL:G:UZ1.M5:U266.L3:-16.611 ps:10 ps:DDR_CTRL_C2C:G:U266.L3:U265.L3:0 ps:10 ps
```

Place 4.7K ohm resistor on top of SM_JUMP3 components so that only pads of SM_JUMP3 are seen.

When assembled 4.7K ohm resistor shall be soldered onto X-B position of jumper as shown.

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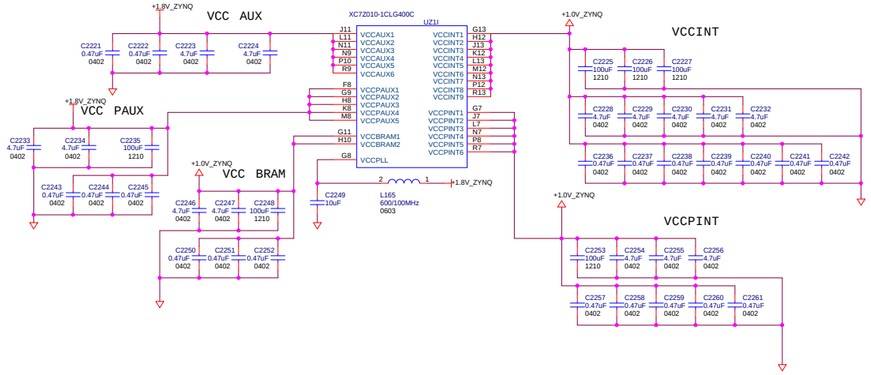
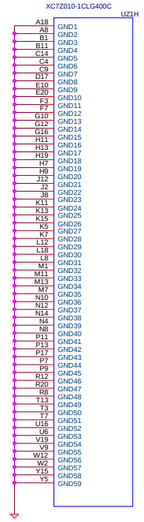
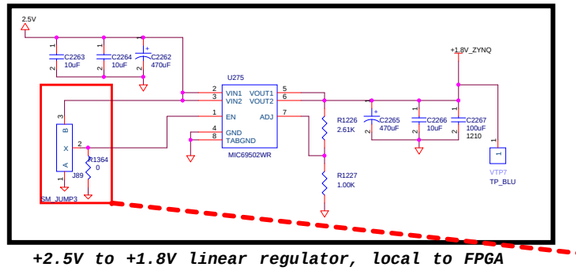
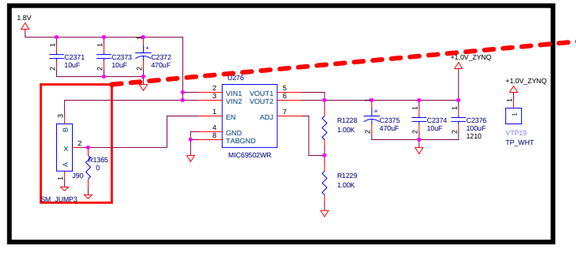






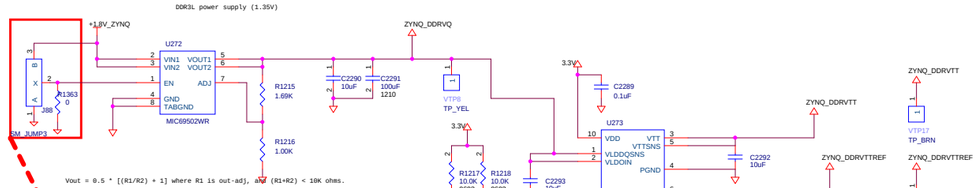
+2.5V to +1.8V linear regulator, local to FPGA



+1.8V to +1.0V linear regulator, local to FPGA

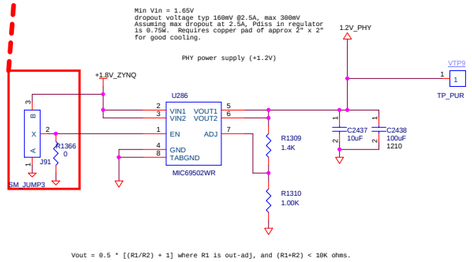
Place 0 ohm resistors on top of SM_JUMP3 components so that only pads of SM_JUMP3 are seen.

When assembled 0 ohm resistors shall be soldered onto A-X or X-B position of jumper as shown.



TPS51206 generates termination voltage VTT from +3.3V.

By definition VTT and VTTREF are set to 1/2 VDDQSNS.



DIP #2) Add SM jumpers to power supplies of Zynq section so that at initial power application regulators are disabled. ANL staff will then move the 0 ohm resistors of the jumpers to the Enable position (X-B) during post-assembly testing.

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