DUNE SiPM Signal Processor(SSP)

DUNE SSP POST-ASSEMBLY Manual Test Procedure

Version 0.1 draft 1 Last Revision 20170412 JTA

Module Serial Number:________________ Testing Date:_________ By:___________

Scope of Procedure

Predecessor Procedure: ***<u>ECO/FCO Verification & initial checkout procedure</u>***

Successor Procedure : ***<u>DUNE SSP Software Mediated Test Procedure.</u>***

The sequence of tests described herein is to be performed on any newly manufactured SSP module after successful completion of the ECO/FCO Verification & initial checkout procedure. Modules with no repair issue sent to ANL solely for firmware upgrade start with this Manual Test Procedure that contains programming of FPGAs.

In every step of this procedure, if a measurement FAILS, immediately stop testing, de-power all circuits, and alert supervising engineer.

Verification of JTAG Chain

Attach JTAG interface dongle to SSP module at connector J66. Connect JTAG dongle to USB port of PC. Start Xilinx's IMPACT program, version 14.7. Turn power to SSP on.

___PASS____ FAIL 1. Verify that the LED of the JTAG dongle is illuminated and green.

___PASS____ FAIL 2. Perform the "initialize chain" function of IMPACT. Verify that *three* devices are identified in the JTAG chain: The ARM processor of the Zynq, the FPGA portion of the Zynq, and the Artix FPGA.

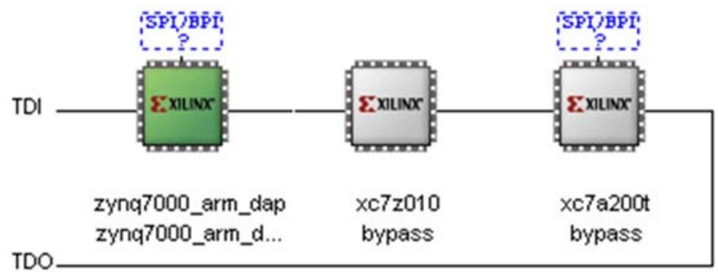

Figure 1 - Expected SSP JTAG chain.

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Program the Zynq's flash RAM using JTAG

___PASS____ FAIL 3. Program the flash RAM image associated with the Zynq FPGA.

____ DONE a. Download the latest version of the Zynq firmware from https://svn.inside.anl.gov/repos/hep_elecdesign/ProtoDune_SSP/Firmware/Communication_FPGA/Trunk/Communication_FPGA.sdk/application/bootimage/BOOT.bin. This is best done by selecting the local working copy of the protoDUNE repository on the local machine and performing an "SVN Update" operation. The typical location that the file is stored locally is C:\SVN_Checkout\ProtoDune_SSP\Firmware\Communication_FPGA\Trunk\Communication_FPGA.sdk\application\bootimage\BOOT.BIN.

____ DONE b. Select the first object in the chain, right-click and select *Add SPI/BPI Flash.* Change the file selection option from the default of **MCS Files (*.mcs)** to **BIN Files (*.bin)**. Browse to the BOOT.BIN file and hit OK. A dialog as shown in Figure 2 will pop up.

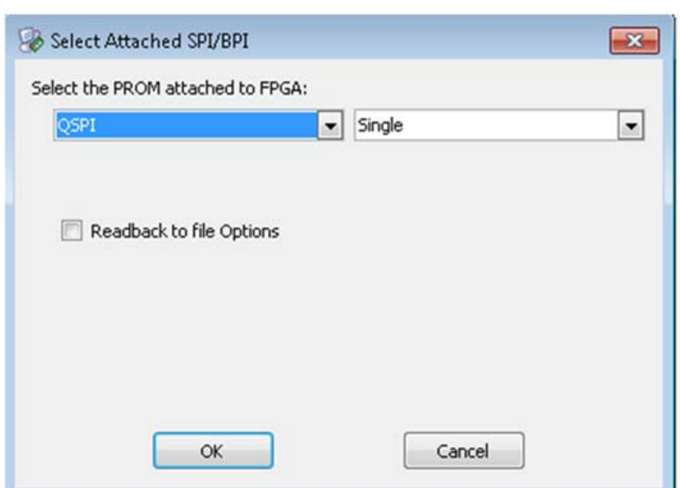

Figure 2 - IMPACT PROM selection screen.

_____ DONE c. Select the options of **QSPI** and **Single** as shown. Hit OK. The image of the chain should change from that shown in Figure 1 to that shown in Figure 3.

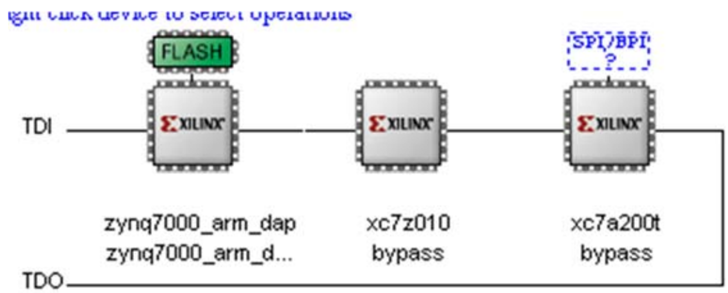

Figure 3 - JTAG chain display after assignment of PROM type

_____ DONE d. Select the **FLASH** object, right-click, and select **Program.**

_____ DONE e. A dialog box should pop up showing progress. After a few minutes the progress bar will get to the end and then a blue & white "success" image should appear.

___PASS____ FAIL 4. Verify that the Zynq processor boots and establishes a physical layer network connection.

_____ DONE a. Insert an SFP modulator into the Ethernet port of the SSP.

_____ DONE b. Verify that the same wavelength of SFP modulator is installed into the fiber optic Ethernet card of the PC.

_____ DONE c. Install a standard LC patch cord from the PC's fiber interface to the fiber interface of the SSP.

_____ DONE d. Cycle the power to the SSP.

_____ DONE e. Verify that the green front panel **LINK** indicator illuminates.

_____ DONE f. Verify that, after a moment, the yellow front panel **LINK** indicator illuminates.

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Perform initial Ethernet access

After cycling power, the Zynq processor should boot up from the newly programmed Flash memory and be able to communicate using Ethernet. Illumination of the two front panel indicators shows that a low-level (physical) connection is present, but data transfers must now be exercised to verify the IP and TCP levels of communication.

___PASS____ FAIL 5. Communication via Ethernet is tested by using the LBNEWare test program.

_____ DONE a. Run LBNEWare. The initial screen as shown in Figure 4 should pop up.

Figure 4 - LBNEWare initial screen.

_____ DONE b. Verify that the **Device IP** is set to the default value of 192.168.1.123.

_____ DONE c. Hit the **Connect** button. The color indicator next to the words *Device Connection* should illuminate red. If the indicator stays black, the test has failed. LBNEWare may throw an error message here after a few seconds if no response is obtained. If this occurs, hit the **Break** button to dismiss the dialog.

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Program Artix FPGA section of Flash RAM using Ethernet

After cycling power, the Zynq processor should boot up from the newly programmed Flash memory and be able to communicate using Ethernet.

___PASS____ FAIL 6. Communication via Ethernet is tested by using the LBNEWare test program.

_____ DONE a. Hit the **Flash** button of the initial LBNEWare screen. The Flash programming window shown in Figure 5 should appear.

_____ DONE b. This screen contains multiple buttons and dialog areas used for different functions. Note that each area is specifically named in Figure 5. These window area names will be referenced in the rest of this section, so make certain to note which is which.

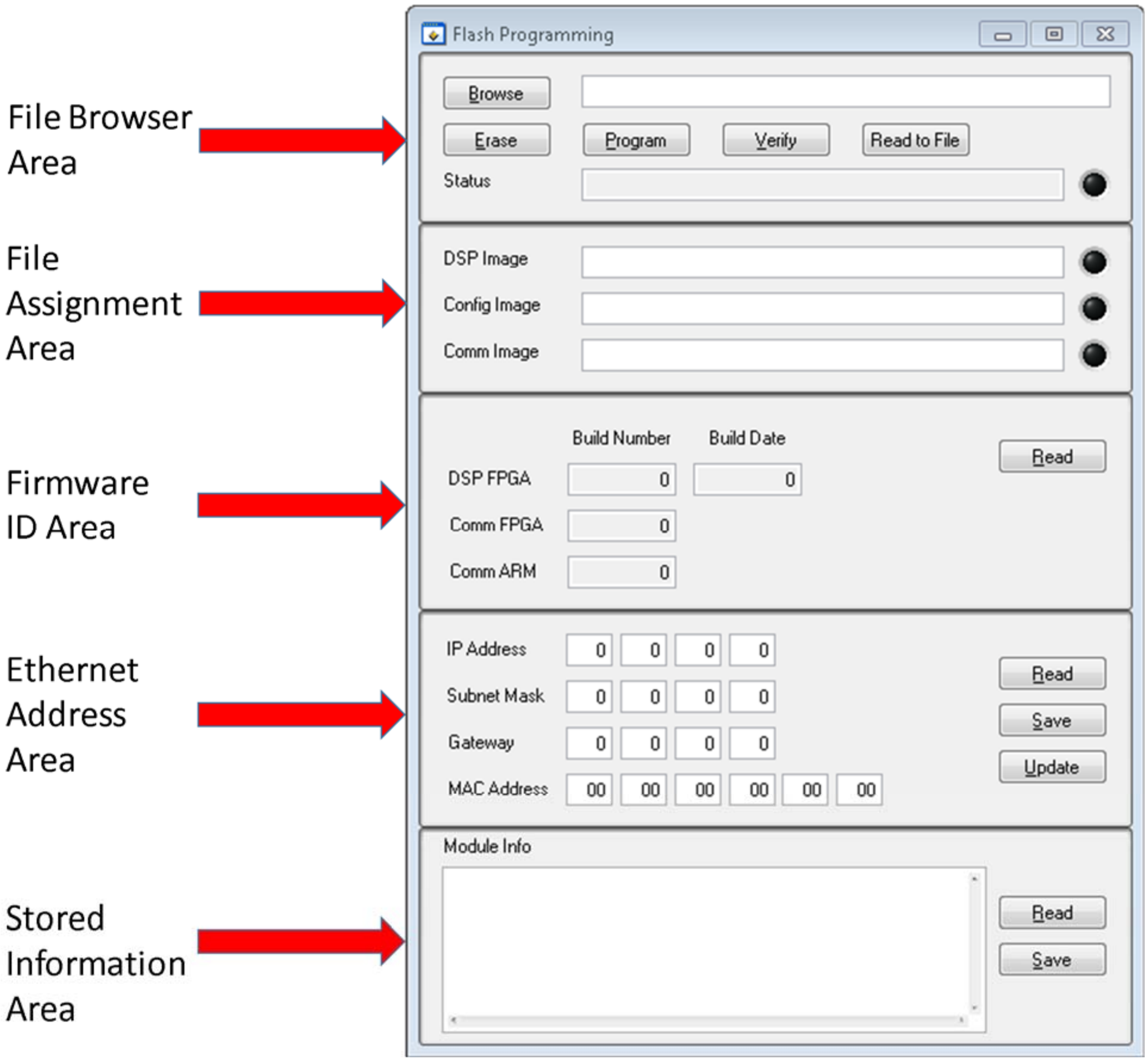

Figure 5 - Flash programming screen.

____ DONE c. In the *Ethernet Address Area* of the Flash Programming window, hit the **Read** button. The IP Address, Subnet mask, Gateway and MAC Address fields should update with the default values expected for a freshly programmed SSP, as shown in Figure 6.

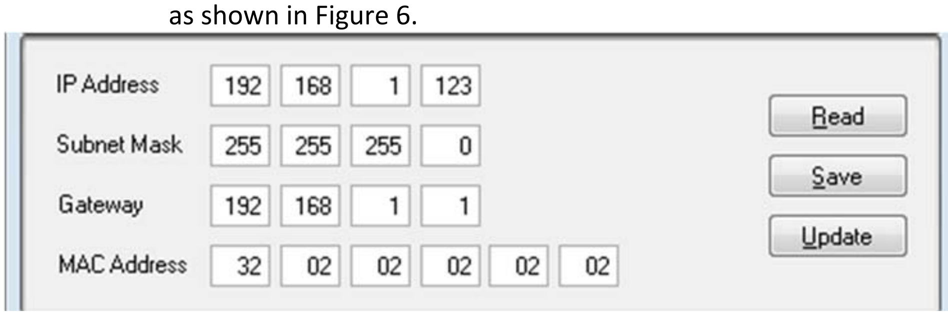

Figure 6 - Default Ethernet settings expected from a freshly programmed SSP

___PASS____ FAIL 7. Verify that all settings read from the module are as shown in Figure 6.

_____ DONE a. IP Address
_____ DONE b. Subnet Mask
_____ DONE c. Gateway
_____ DONE d. MAC address

___PASS____ FAIL 8. Program the Artix FPGA ram area.

_____ DONE a. Download the latest version of the DSP FPGA firmware image from SVN to the computer's local hard drive.

_____ DONE b. Use the *File Browser* control to select the current version of the DSP FPGA firmware image downloaded in step 8a above.

_____ DONE c. Copy/paste the full path from the Browse box to the DSP Image box in the *Firmware Assignment* area.

_____ DONE d. Click the radio button to the right of the DSP Image box to make it red.

_____ DONE e. Ensure that the radio buttons to the right of the Config Image and Comm Image boxes are black.

_____ DONE f. Hit the Erase button. Verify erasure completes without error.

_____ DONE g. Hit the Program button. Verify programming cycle completes without error.

_____ DONE h. Hit the Verify button. Verify that procedure completes with no errors.

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Final Check after reprogramming module

After cycling power, the Zynq processor should boot up from the newly programmed Flash memory, then boot the Artix FPGA and be able to communicate with the Artix FPGA. Reading a set of registers from both devices verifies this to be the case.

___PASS____ FAIL 9. Verify correct operation of front panel LEDs.

_____ DONE a. Cycle power to SSP.

_____ DONE b. Examine front panel of SSP as power is turned on. Compare against Figure 7. The Link LED will come on after a short delay.

Figure 7 - Front panel of SSP after programming of FPGAs

___PASS____ FAIL 10. Verify that communication with module still works by reading the *Firmware ID* values from the device.

_____ DONE a. Close LBNEWare.

_____ DONE b. Restart LBNEWare.

_____ DONE c. Re-establish communication with SSP.

_____ DONE d. Record DSP FPGA build number : ___________________________

____ DONE e. Record DSP FPGA build date: ______________________________

____ DONE f. Record Comm FPGA build number : _________________________

____ DONE g. Record Comm ARM build number : _________________________

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