DUNE SiPM Signal Processor(SSP)

Overview of Post-Assembly and Characterization testing methodology

Version 1.2 Last Revision 20170717 JTA

Introduction

The SiPM Signal Processor, or SSP module, undergoes a series of tests after a new board is received from the assembler to verify operation and performance, as described in the document **Quality Assurance and Control for the ProtoDUNE-SP Photon Detector Readout Electronics** dated April 5, 2017. That document describes five different overall phases of testing named *Post-Assembly, Characterization, Vertical Slice, Integration* and *Installation.* This document provides a more detailed breakdown of the *Post-Assembly* and *Characterization* stages of testing, specifically to highlight the flowchart of sub-tasks within these testing regimes and also to clearly define the type and scope of QA/QC documentation that is generated at each step.

Specific Flowchart of the Post-Assembly testing phase

During the Post-Assembly test phase a newly manufactured SSP module is inspected, updated with any component or circuit changes that have been approved since the release of the Bill of Materials to the assembler, verified to work at a basic level and loaded with firmware. The Post-Assembly testing phase has been sub-divided into a series of procedures, defined by the level of automation that can be applied and the method of recording data obtained during that procedure. A given module must pass a given procedure completely prior to progressing to the next procedure.

Test procedure	***Type of QA/QC documentation***	***Level of automation***
ECO/FCO verification and initial checkout	Paper, written by technician, saved in “traveler” binder	None. Performed on technician bench without computer present.
Post-assembly manual test procedure	Paper, written by technician, saved in “traveler” binder	Computer used by technician but all data is recorded manually as communication with module by test stand software is not yet present.
Software mediated test procedure	Data files saved by software	Partial. Software controls module and records results but technician is required to connect/disconnect external cables and test equipment.
Automated test procedure	Data files saved by software	Full. Tests run without human supervision after startup.

Recording of QA/QC information

During the ECO/FCO verification and post-assembly manual test procedures, a human-readable document is provided on paper with various places to record the operator, date, module serial number and results of tests. For each task enumerated in the document the technician is required to indicate that each task is performed and provide a general pass/fail indication. The procedure is sub-divided into sections, and the technician is required to sign and date when a module passes all criteria listed for that section. The filled-in papers with technician signature are stored in folders, one per module serial number.

During the software mediated and automated test procedures, the test stand software records all relevant data, statistics and pass-fail criteria in files that are keyed by serial number and date. The file structure and details of format for each file are described in the separate **ProtoDUNE SSP software test plan** document. A simplistic summary of that document is that all module test history is stored in a combination of summary and raw data files, keyed by module serial number, that are saved locally to the computer during the process of testing and backed up to a cloud drive as each testing step is completed.

Summary of tests performed by each procedure

This section provides a quick summary of what features/functions of the SSP are exercised by each test procedure enumerated above.

ECO/FCO verification and initial checkout

Overall, this procedure verifies the construction of the SSP. The specific operations included in this procedure are

1. Visual inspection of PCB assembly including
    a. Attachment of serial number
    b. Installation of EMI shields
    c. Installation of board into chassis
    d. Installation of heat sinks
    e. Modifications to component values and/or circuit topology as defined in approved Fabrication Change Order (FCO) and Engineering Change Order (ECO) documents.
2. Ohm-meter measurements of various test points to check for power supply shorts and repair of any aberrations detected.
3. Volt-meter and oscilloscope measurements of module internal power supplies with supplies disconnected from FPGAs and analog circuitry; adjustment if needed of any voltages.
4. Installation of components to connect verified power supplies to rest of design.
5. Re-verification of all power supplies with loads connected.
6. Check of external bias supply connection.

Manual Test Procedure

The Manual test procedure assumes that the power supplies of the SSP are functional and continues with programming of the FPGAs, checks of static analog performance, exercising physical

interfaces and verification of all indicators. Upon successful completion of this procedure the SSP can be controlled and read out using software. The specific operations included in this procedure are

1. Verify JTAG chain.
2. Perform initial programming of Flash RAM over JTAG.
3. Perform initial Ethernet access test.
4. Use Ethernet to program rest of Flash RAM
5. Record build number/build date of firmware images as read from module over Ethernet.

Software Mediated Test Procedure

The Software Mediated Test procedure assumes that the device under test is capable of Ethernet communication and has firmware loaded into all programmable devices. These tests utilize software to perform measurements and, where possible, to calculate pass/fail results, but require significant human interaction to move cables, visually verify indicators, etc. Upon successful completion of this procedure the module is considered generally functional. The specific operations included in this procedure are

1. Blink all firmware-controlled LED indicators
2. Verify operation of Trig Out and Reset In fiber optic connections
3. Verify ADC clock stability and phase.
4. Verify basic FADC operation, noise and DC offset.
5. Use external pulser to verify connectivity through RJ45 connectors.
6. Verify base operation of monitoring ADC functions.
7. Qualitatively verify operation of charge injection circuitry.
8. Verify bias voltage output.
9. Response of SSP to timing system commands
    a. Currently this is a limited test but is expected to expand as more software for the timing system emulator becomes available.

Automated Test Procedure

The Software Mediated Test procedure assumes that the device under test has passed the Software Mediated Test Procedure. The only human interaction within these tests is initial setup of cabling or connections, but all measurement is performed by software. The specific operations included in this procedure are

1. Complete charge injection (QI) scan with linearity/gain/offset checks
2. G.E.T.S. block detailed operation
3. System temperature monitors
4. Full bias voltage output, bias voltage and bias current monitoring circuit scan

Current status of test procedures

Procedure Name	***Status as of 20170717***
ECO/FCO verification and initial checkout	Paper document complete. Has been used on all modules of mini-production.
Manual Test Procedure	Paper document complete. Is being used on modules of mini-production.
Software Mediated Test Procedure	All tests possible by experienced user of LBNEWare. Technician/student friendly version in development.
Automated Test Procedure	Software in development.