

1 DUNE Far Detector Timing and Synchronization System

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1 0.1 Introduction

2 All components of the far detector (FD) are driven with clocks derived from a single GPS disciplined
3 source. Components of the SP module are synchronized to a 62.5 MHz clock. Components of the
4 DP module are synchronized to a 125 MHz.

5 In order to make full use of the information from the photon detection system (PDS), the common
6 clock must be aligned within a single detector unit with an accuracy of O 1ns. In order to form a
7 common trigger for supernova neutrino burst (SNB) between detector modules, the timing between
8 them must be aligned with an accuracy of O 1ms. However, a tighter constraint is the need to
9 calibrate the common clock to universal time (derived from GPS) in order to adjust the data
10 selection algorithm inside an accelerator spill, which requires an absolute accuracy of O 1 μ s.

11 SP and DP detector modules use different timing systems, driven by the different technical re-
12 quirements and development history of the two technologies. A SP module has many more timing
13 end points than a DP module and many of the end points are simpler than the end points in
14 the DP, for example a warm interface board (WIB) versus Micro Telecommunications Computing
15 Architecture (μ TCA) crate. Both systems have been successfully prototyped.

16 0.2 Single Phase

17 The DUNE SP module uses a development of the ProtoDUNE-SP timing system. Synchronization
18 messages are transmitted over a serial data stream with the clock embedded in the data. The format
19 is described in DUNE DocDB-1651 [?]. Figure 1 shows the overall arrangement of components
20 within the Single Phase Timing System (SPTS) A stable master clock, disciplined with a 10 MHz
21 reference is used in the SPTS. An Inter-range instrumentation group time code (IRIG) signal is
22 also received by the system and used to set the SPTS 64-bit time-stamp. However the periodic
23 synchronization messages distributed to the single-phase (SP) detector module are an exact number
24 of clock cycles apart even if there is jitter in the IRIG signal.

25 The GPS signal is encoded onto optical fiber and transmitted to the central utility cavern (CUC),
26 where it is converted back to an RF signal on coaxial cable and used as the input to a GPS
27 disciplined oscillator. The oscillator module also houses a IEEE 1588 (PTP) grandmaster and an
28 NTP server. The PTP grandmaster provides a timing signal for the dual-phase (DP) White Rabbit
29 (WR) timing network. The NTP server provides an absolute time for the one-pulse-per-second
30 signal (1PPS signal). The SPTS relates its time counter onto GPS time by timestamping the 1PPS
31 signal onto the SPTS time counter and reading the time in software from the NTP server.

32 The latency from the GPS antenna on the surface to the Dune Timing System (DTS) master in
33 the CUC will be compensated for by measuring the round trip delay over a single mode fibre in
34 the same bundle at the raw GPS signal coming from the antenna.

35 The WR synchronization signals from the DP detector module are time-stamped onto the SPTS

- 1 clock domain and the SPTS synchronization signals are time stamped onto the DP clock domain.
- 2 This allows the timing in the SP and DP detector modules to be aligned. A similar scheme is used
- 3 to relate the ProtoDUNE-SP timing domain to the beam instrumentation WR time domain.

- 4 In order to provide redundancy, and also the ability to easily detect issues with the timing path,
- 5 two independent GPS systems are used. One with an antenna at the head of the Yates Shaft,
- 6 the other with an antenna at the head of the Ross Shaft. The two independent timing paths are
- 7 brought together in the same rack in the CUC. Using 1:2 fibre splitters one SPTS unit can be left
- 8 as a hot spare while the other is active. This also allows testing of new firmware and software
- 9 during comissioning without the risk of losing the SPTS if a bug is introduced.

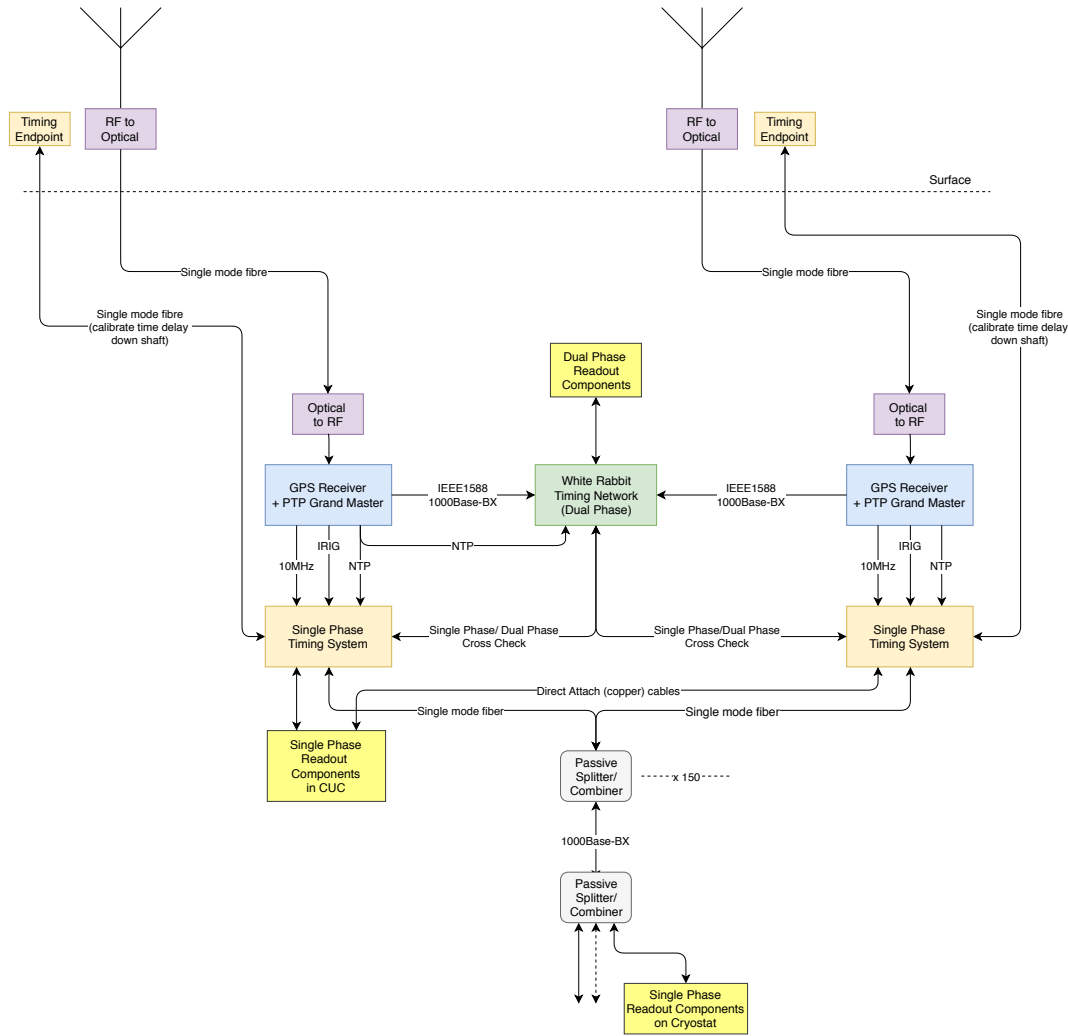


Figure 1: Illustration of the components in the DUNE timing system.

- 10 All the custom electronic components for the SPTS are contained in two μ TCA shelves. At any
- 11 one time one is active and the other is a hot spare. The 10 MHz reference clock and the 1PPS signal
- 12 are received by a single width advanced mezzanine card (AMC) at the center of the μ TCA shelf.
- 13 This master timing AMC is a custom board and produces the SPTS signals and encodes them onto
- 14 a serial data stream. This serial datastream is distributed over a standard star-point backplane to
- 15 each of the fanout AMC. The fanout AMC is an off-the-self board, probably the ohwr.org hosted

1 "AMC FMC Carrier" design, carrying two custom FPGA Mezzanine Card (FMC). Each FMC has
 2 four SFP cages. The SFP cages are either occupied by 1000Base-BX SFPs, each of which connects
 3 to a fiber running to an anode plane assembly (APA), or to a Direct Attach cable which connects
 4 to systems elsewhere in the CUC. This arrangement is shown in Figure 2

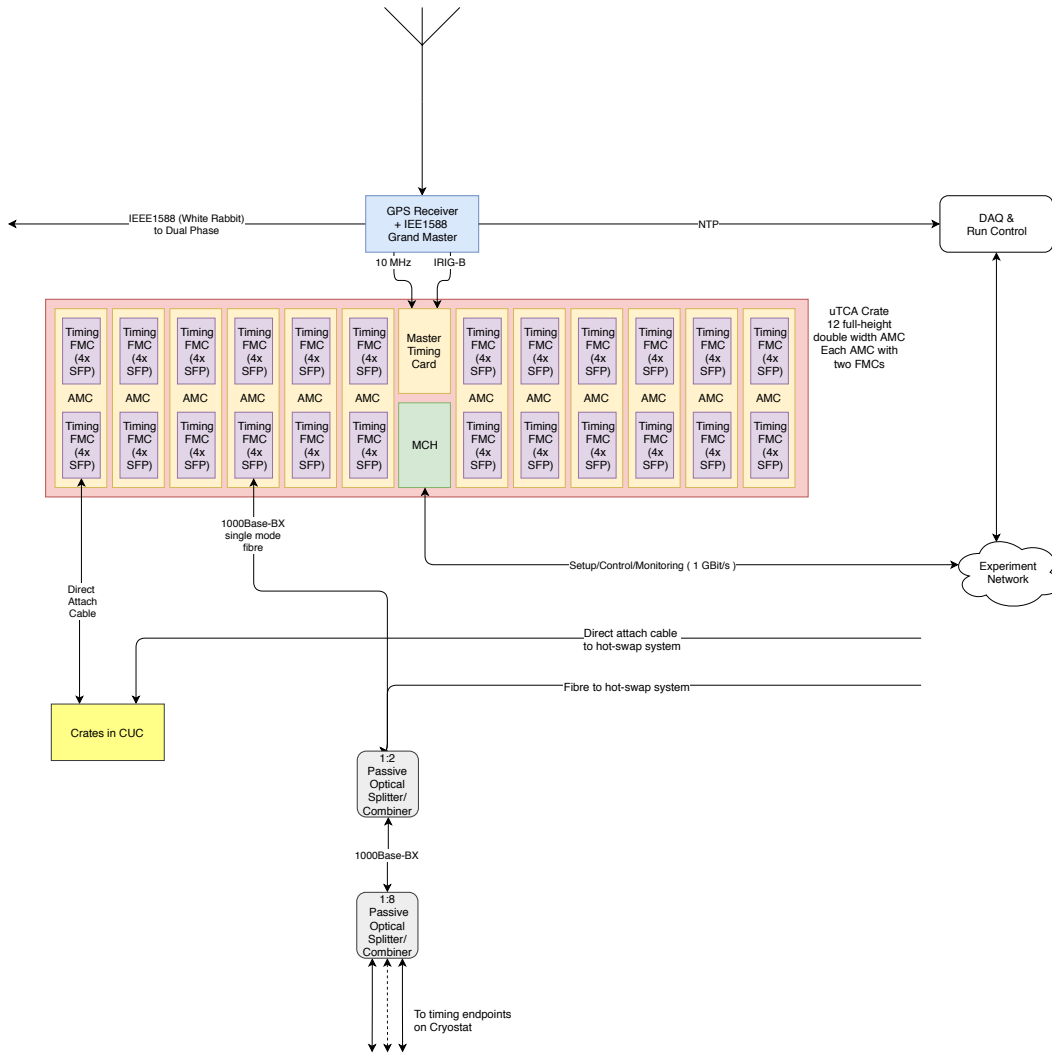


Figure 2: Illustration of the components in the SP timing system.

5 0.2.1 Commissioning

6 The DTS will be one of the first DAQ components installed in the CUC so that timing and
 7 synchronization signals are available the other components of the DAQ as soon as they start to
 8 be installed. Early in the construction project SPTS “development kits” will be made available.
 9 The kits will include the hardware and software needed to produce SPTS timing signal. This will
 10 allow the teams developing the DUNE readout systems to integrate with the SPTS early in the
 11 development process. Hardware and software will also be available for use in vertical slice tests
 12 and the integration and test facility (ITF).

1 0.3 Dual Phase

2 The DP module uses the WR implementation of the IEEE1588-2008 timing distribution standard.
3 The components that distribute the timing signals are included in the scope of the DP readout
4 electronics and are not described here. The interface between the DTS and the DP readout
5 electronics is by means of 1000Base-BX Small form-factor pluggable transceiver (SFP) coupled by
6 single mode fibre. There will be two fibres carrying IEEE1588-2008 timing signals supplied to the
7 DP readout electronics, one from each of the two GPS receivers.

8 0.3.0.1 Beam timing

9 The neutrino beam is produced at the Fermilab accelerator complex in spills of $10\ \mu\text{s}$ duration. A
10 spill location system (SLS) at the Far Detector site will locate the time periods in the data when
11 beam could be present, based on network packets received from Fermilab containing predictions
12 of the GPS-time of spills soon to occur or absolute time stamps of recent spills. Experience from
13 MINOS and $\text{NO}\nu\text{A}$ shows that this can provide beam triggering with high reliability with some
14 small fraction of late or dropped packets. To improve reliability further, the system outlined here
15 contains an extra layer of redundancy in the prediction process. Several stages of prediction based
16 on recent spill behavior will be applied, aiming for an accuracy of better than 10% of a readout time
17 (sub-ms) in time for the data to be selected from the data acquisition (DAQ) buffers. Ultimately,
18 an offline database will match the actual time of the spill with the data, thus removing any reliance
19 on real-time network transfer for this crucial stage of the oscillation measurements. The network
20 transfer of spill-timing information is simply to ensure that a correctly located and sufficiently
21 wide window of data is considered as beam data. This system is not required, and is not designed
22 to provide signals accurate enough to measure neutrino time-of-flight.

23 The precision to which the spill time can be predicted at Fermilab improves as the acceleration
24 process of the protons producing the spill in question advances. The spills currently occur at
25 intervals of 1.3s; the system will be designed to work with any interval, and to be adaptable in
26 case the sequence described here changes. For redundancy, three packets will be sent to the far
27 detector for each spill. The first is approximately 1.6s before the spill-time, which is at the point
28 where a 15 Hz booster cycle is selected; from this point on, there will be a fixed number of booster
29 cycles until the neutrinos and the time is subject to a few ms of jitter. The second is about 0.7s
30 before the spill, at the point where the main injector acceleration is no longer coupled to the
31 booster timing; this is governed by a crystal oscillator and so has a few μs of jitter. The third
32 will be at the so called ‘\$74’ signal generated before the beamline kicker magnet fires to direct the
33 protons at the LBNF target; this doesn’t improve the timing at the Far Detector much, but serves
34 as a cross check for missing packets. This system is enhanced compared to that of MINOS- $\text{NO}\nu\text{A}$,
35 which only use a third of the above timing signals. The reason for the larger uncertainty in the
36 time interval from 1.6s to 0.7s is that the booster cycle time is synchronized to the electricity
37 supply company’s 60 Hz, which has a variation of about 1%.

38 Arrival-time monitoring information from a year of MINOS data-taking was analyzed, and it was
39 found that 97% of packets arrived within 100 ms of being sent and 99.88% within 300 ms.

1 The SLS will therefore have estimators of the GPS-times of future spills, and recent spills with
2 associated data contained in the DAQ primary buffers (primary buffers). These estimators will
3 improve in precision as more packets arrive. The DAQ will use data in a wider window than usual,
4 if, at the time the trigger decision has to be made, the precision is lower due to missing or late
5 packets. From the MINOS monitoring analysis, this is expected to be very rare.