Created: 13Sep2016
Updated: 09/20/2017 (no change for RCE from 08/02/2017)
Version: 1.1-rc2-RCE

	K/D	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6
1	0001	Reserved (8)								SlotNo				CrateNo				FiberNo				Version = 0x1					
2	0000	WIB Errors																Reserved (14)									
3	0000	Timestamp [31:0]																									
4	0000	Z	Timestamp [62:48] or WIB counter [3]																							Timestamp [47:32]	
5	0000	ChkSm B [7:0]								ChkSm A [7:0]								Reserved (8)								Stream	
6	0000	COLDDATA Convert Count																ChkSm B [15:8]									
7	0000	Reserved																								Error Register	
8	0000	HDR8						HDR6					HDR7					HDR5				HDR4				HDR2			HD
9	0000	ADC2 CH2[3:0]				ADC2 CH1[11:8]				ADC1 CH2[3:0]				ADC1 CH1[11:8]				ADC2 CH1[7:0]									
10	0000	ADC2 CH3[7:0]								ADC1 CH3[7:0]								ADC2 CH2[11:4]									
11	0000	ADC2 CH4[11:4]								ADC1 CH4[11:4]								ADC2 CH4[3:0]				ADC2 CH3[11:8]				ADC1 CI	
12	0000	ADC2 CH6[3:0]				ADC2 CH5[11:8]				ADC1 CH6[3:0]				ADC1 CH5[11:8]				ADC2 CH5[7:0]									
13	0000	ADC2 CH7[7:0]								ADC1 CH7[7:0]								ADC2 CH6[11:4]									
14	0000	ADC2 CH8[11:4]								ADC1 CH8[11:4]								ADC2 CH8[3:0]				ADC2 CH7[11:8]				ADC1 CI	
15	0000	ADC4 CH2[3:0]				ADC4 CH1[11:8]				ADC3 CH2[3:0]				ADC3 CH1[11:8]				ADC4 CH1[7:0]									
16	0000	ADC4 CH3[7:0]								ADC3 CH3[7:0]								ADC4 CH2[11:4]									
17	0000	ADC4 CH4[11:4]								ADC3 CH4[11:4]								ADC4 CH4[3:0]				ADC4 CH3[11:8]				ADC3 CI	
18	0000	ADC4 CH6[3:0]				ADC4 CH5[11:8]				ADC3 CH6[3:0]				ADC3 CH5[11:8]				ADC4 CH5[7:0]									
19	0000	ADC4 CH7[7:0]								ADC3 CH7[7:0]								ADC4 CH6[11:4]									
20	0000	ADC4 CH8[11:4]								ADC3 CH8[11:4]								ADC4 CH8[3:0]				ADC4 CH7[11:8]				ADC3 CI	
21	0000	ADC6 CH2[3:0]				ADC6 CH1[11:8]				ADC5 CH2[3:0]				ADC5 CH1[11:8]				ADC6 CH1[7:0]									

22	0000	ADC6 CH3[7:0]						ADC5 CH3[7:0]						ADC6 CH2[11:4]		
23	0000	ADC6 CH4[11:4]						ADC5 CH4[11:4]						ADC6 CH4[3:0]	ADC6 CH3[11:8]	ADC5 CH
24	0000	ADC6 CH6[3:0]		ADC6 CH5[11:8]				ADC5 CH6[3:0]		ADC5 CH5[11:8]				ADC6 CH5[7:0]		
25	0000	ADC6 CH7[7:0]						ADC5 CH7[7:0]						ADC6 CH6[11:4]		
26	0000	ADC6 CH8[11:4]						ADC5 CH8[11:4]						ADC6 CH8[3:0]	ADC6 CH7[11:8]	ADC5 CH
27	0000	ADC8 CH2[3:0]		ADC8 CH1[11:8]				ADC7 CH2[3:0]		ADC7 CH1[11:8]				ADC8 CH1[7:0]		
28	0000	ADC8 CH3[7:0]						ADC7 CH3[7:0]						ADC8 CH2[11:4]		
29	0000	ADC8 CH4[11:4]						ADC7 CH4[11:4]						ADC8 CH4[3:0]	ADC8 CH3[11:8]	ADC7 CH
30	0000	ADC8 CH6[3:0]		ADC8 CH5[11:8]				ADC7 CH6[3:0]		ADC7 CH5[11:8]				ADC8 CH5[7:0]		
31	0000	ADC8 CH7[7:0]						ADC7 CH7[7:0]						ADC8 CH6[11:4]		
32	0000	ADC8 CH8[11:4]						ADC7 CH8[11:4]						ADC8 CH8[3:0]	ADC8 CH7[11:8]	ADC7 CH
33	0000	ChkSm B [7:0]						ChkSm A [7:0]						Reserved (8)		Stream

34	0000	COLDDATA Convert Count												ChkSm B [15:8]		
35	0000	Reserved													Error Register	
36	0000	HDR8		HDR6		HDR7		HDR5		HDR4		HDR2				HD
37	0000	ADC2 CH2[3:0]		ADC2 CH1[11:8]		ADC1 CH2[3:0]		ADC1 CH1[11:8]		ADC2 CH1[7:0]						
38	0000	ADC2 CH3[7:0]				ADC1 CH3[7:0]				ADC2 CH2[11:4]						
39	0000	ADC2 CH4[11:4]				ADC1 CH4[11:4]				ADC2 CH4[3:0]	ADC2 CH3[11:8]					ADC1 CH
40	0000	ADC2 CH6[3:0]		ADC2 CH5[11:8]		ADC1 CH6[3:0]		ADC1 CH5[11:8]		ADC2 CH5[7:0]						
41	0000	ADC2 CH7[7:0]				ADC1 CH7[7:0]				ADC2 CH6[11:4]						
42	0000	ADC2 CH8[11:4]				ADC1 CH8[11:4]				ADC2 CH8[3:0]	ADC2 CH7[11:8]					ADC1 CH
43	0000	ADC4 CH2[3:0]		ADC4 CH1[11:8]		ADC3 CH2[3:0]		ADC3 CH1[11:8]		ADC4 CH1[7:0]						
44	0000	ADC4 CH3[7:0]				ADC3 CH3[7:0]				ADC4 CH2[11:4]						
45	0000	ADC4 CH4[11:4]				ADC3 CH4[11:4]				ADC4 CH4[3:0]	ADC4 CH3[11:8]					ADC3 CH
46	0000	ADC4 CH6[3:0]		ADC4 CH5[11:8]		ADC3 CH6[3:0]		ADC3 CH5[11:8]		ADC4 CH5[7:0]						
47	0000	ADC4 CH7[7:0]				ADC3 CH7[7:0]				ADC4 CH6[11:4]						
48	0000	ADC4 CH8[11:4]				ADC3 CH8[11:4]				ADC4 CH8[3:0]	ADC4 CH7[11:8]					ADC3 CH

49	0000	ADC6 CH2[3:0]	ADC6 CH1[11:8]	ADC5 CH2[3:0]	ADC5 CH1[11:8]	ADC6 CH1[7:0]		
50	0000	ADC6 CH3[7:0]		ADC5 CH3[7:0]		ADC6 CH2[11:4]		
51	0000	ADC6 CH4[11:4]		ADC5 CH4[11:4]		ADC6 CH4[3:0]	ADC6 CH3[11:8]	ADC5 C
52	0000	ADC6 CH6[3:0]	ADC6 CH5[11:8]	ADC5 CH6[3:0]	ADC5 CH5[11:8]	ADC6 CH5[7:0]		
53	0000	ADC6 CH7[7:0]		ADC5 CH7[7:0]		ADC6 CH6[11:4]		
54	0000	ADC6 CH8[11:4]		ADC5 CH8[11:4]		ADC6 CH8[3:0]	ADC6 CH7[11:8]	ADC5 C
55	0000	ADC8 CH2[3:0]	ADC8 CH1[11:8]	ADC7 CH2[3:0]	ADC7 CH1[11:8]	ADC8 CH1[7:0]		
56	0000	ADC8 CH3[7:0]		ADC7 CH3[7:0]		ADC8 CH2[11:4]		
57	0000	ADC8 CH4[11:4]		ADC7 CH4[11:4]		ADC8 CH4[3:0]	ADC8 CH3[11:8]	ADC7 C
58	0000	ADC8 CH6[3:0]	ADC8 CH5[11:8]	ADC7 CH6[3:0]	ADC7 CH5[11:8]	ADC8 CH5[7:0]		
59	0000	ADC8 CH7[7:0]		ADC7 CH7[7:0]		ADC8 CH6[11:4]		
60	0000	ADC8 CH8[11:4]		ADC7 CH8[11:4]		ADC8 CH8[3:0]	ADC8 CH7[11:8]	ADC7 C
61	0000	CRC-32 [31:0]						
62	0000	K28.2		K28.1		K28.2		
63	0000	NEXT FRAME				K28.2		

5	4	3	2	1	0	Data Source	Notes
SOF						WIB	SOF is K28.5(0xBC) Format version currently = 1.
				OOS	MM	WIB	OOS: bad syncs coming from the PDTS. MM: COLDATA convert counters don't match
						WIB	
						WIB	Bits [30:16] of word 3 may be either the upper 8 bits of the timestamp or a WIB debug counter Bit 31 ('Z') of word 3 = WIB-CD1
ı 2 ERR				Stream 1 ERR		COLDATA 1/WIB	16 bit frame checksum will be calculated for each 8 bit wide stream to serializers. 16 bit counter; increments with 2 MHz ADC Covert; resets with SYNC
ChkSm A [15:8]						COLDATA 1	
						COLDATA 1	Reports alignment errors on input streams; TBD
R3			HDR1			COLDATA 1	Header Bits
ADC1 CH1[7:0]						COLDATA 1	
ADC1 CH2[11:4]						COLDATA 1	
H4[3:0]		ADC1 CH3[11:8]				COLDATA 1	
ADC1 CH5[7:0]						COLDATA 1	
ADC1 CH6[11:4]						COLDATA 1	
H8[3:0]		ADC1 CH7[11:8]				COLDATA 1	
ADC3 CH1[7:0]						COLDATA 1	
ADC3 CH2[11:4]						COLDATA 1	
H4[3:0]		ADC3 CH3[11:8]				COLDATA 1	
ADC3 CH5[7:0]						COLDATA 1	
ADC3 CH6[11:4]						COLDATA 1	
H8[3:0]		ADC3 CH7[11:8]				COLDATA 1	
ADC5 CH1[7:0]						COLDATA 1	

ADC5 CH2[11:4]		COLDATA 1	
H4[3:0]	ADC5 CH3[11:8]	COLDATA 1	
ADC5 CH5[7:0]		COLDATA 1	
ADC5 CH6[11:4]		COLDATA 1	
H8[3:0]	ADC5 CH7[11:8]	COLDATA 1	
ADC7 CH1[7:0]		COLDATA 1	
ADC7 CH2[11:4]		COLDATA 1	
H4[3:0]	ADC7 CH3[11:8]	COLDATA 1	
ADC7 CH5[7:0]		COLDATA 1	
ADC7 CH6[11:4]		COLDATA 1	
H8[3:0]	ADC7 CH7[11:8]	COLDATA 1	
ı 2 ERR	Stream 1 ERR	COLDATA 2/WIB	WIB-CD2
			16 bit frame checksum will be calculated for each 8 bit wide stream to serializers. 16 bit counter; increments with 2 MHz ADC Covert; resets with
ChkSm A [15:8]		COLDATA 2	SYNC
		COLDATA 2	Reports alignment errors on input streams; TBD
R3	HDR1	COLDATA 2	Header Bits
ADC1 CH1[7:0]		COLDATA 2	
ADC1 CH2[11:4]		COLDATA 2	
H4[3:0]	ADC1 CH3[11:8]	COLDATA 2	
ADC1 CH5[7:0]		COLDATA 2	
ADC1 CH6[11:4]		COLDATA 2	
H8[3:0]	ADC1 CH7[11:8]	COLDATA 2	
ADC3 CH1[7:0]		COLDATA 2	
ADC3 CH2[11:4]		COLDATA 2	
H4[3:0]	ADC3 CH3[11:8]	COLDATA 2	
ADC3 CH5[7:0]		COLDATA 2	
ADC3 CH6[11:4]		COLDATA 2	
H8[3:0]	ADC3 CH7[11:8]	COLDATA 2	

ADC5 CH1[7:0]		COLDATA 2	
ADC5 CH2[11:4]		COLDATA 2	
H4[3:0]	ADC5 CH3[11:8]	COLDATA 2	
ADC5 CH5[7:0]		COLDATA 2	
ADC5 CH6[11:4]		COLDATA 2	
H8[3:0]	ADC5 CH7[11:8]	COLDATA 2	
ADC7 CH1[7:0]		COLDATA 2	
ADC7 CH2[11:4]		COLDATA 2	
H4[3:0]	ADC7 CH3[11:8]	COLDATA 2	
ADC7 CH5[7:0]		COLDATA 2	
ADC7 CH6[11:4]		COLDATA 2	
H8[3:0]	ADC7 CH7[11:8]	COLDATA 2	
		WIB	
K28.1		IDLE	
K28.1		IDLE	One half 32bit word (RCE format is a multiple of 16bits, not 32, so it wraps on the 32 bit boundary)

of word 3 = '0' for full timestamp mode (63 bit timestamp) or '1' for WIB counter mode